

2.64 Gbit/s Full-Duplex Serial Link - Piggyback Board

The GigaSTaR[®] piggyback board ING_TRC represents an easy-to-use implementation of a full-duplex GigaSTaR[®] High-Speed link with 2.64 Gbit/s (330 Mbyte/s) bandwidth.

Equipped with the GigaSTaR[®] Transmitter- and Receiver devices INGT165B/INGR165B and a few external components, the board offers all the functionality to be directly connected to a plain 2x36bit, 33 MHz parallel Interface through a compact 140 pin connector. The duplex high-speed serial signals are available at a SUB D9 connector which is directly mounted on the piggyback board. The pinout is compatible to industry-standard Shielded-Twisted-Pair (STP) cables. With the compact size of 64 x 59 mm and a variable distance of 6-14 mm to the main board, this piggyback can be easily adapted to any system environment.

The GigaSTaR[®] piggyback board is available in a full-duplex version with a native copper-cable interface ING_TRC. For information on the dual transmitter/receiver version see the ING_TTC datasheet. For information on the piggyback board with fiber-optic interface see the ING_TRF datasheet.

The piggyback boards also can be combined with the GigaSTaR[®] Application Kit ING_AK to build a full-duplex, serial high-speed link for fast prototyping and evaluation purposes.

Technical details on the GigaSTaR[®] Transmitter- and Receiver-devices INGT165B/INGR165B are available in the product datasheet ING165B_DS.

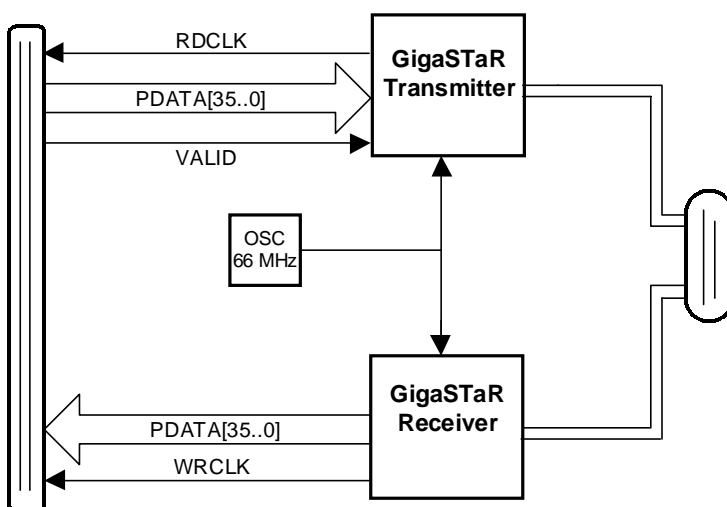


Figure 1: Piggyback Board functional schematics

GigaSTaR[®] Piggyback Board ING_TRC

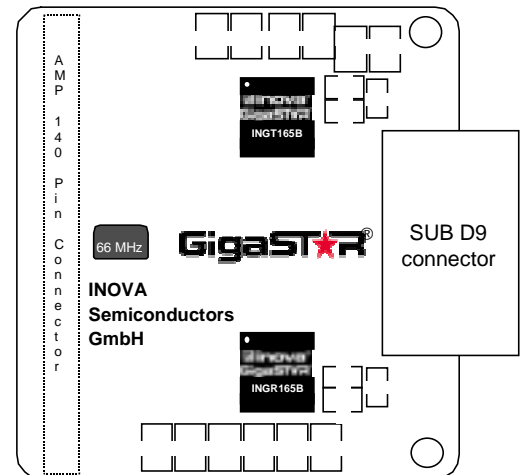


Figure 2: Original size of the piggyback board

FEATURES

- Compact size of 64 x 59 mm
- Full-duplex 297 Mbyte/s payload data rate (sustained)
- Parallel Tx/Rx-Interfaces (each 36 bit @ 33 MHz)
- Mounted SUB D9 receptacle for connection to Shielded Twisted Pair Cable (Gore part # : GGSC1608-X)
- 140 pin, 0.8 mm pitch Free-Height Connector (AMP part #179029-6 for selectable height receptacles: 6/10/14 mm board spacing)
- On-board reference-clock (prepared for optional external clock)
- Full AC-coupling to the serial link cable (100nF, 50 V capacitors)
- Multilayer board for highest EMI-immunity
- Single 3.3 V DC-supply

1. GigaSTaR[®] LINK DESCRIPTION

The GigaSTaR[®] link is designed for reliable high-speed, low-latency data transmissions. All functions for the data transfer management, including the high-frequency blocks are fully integrated in the Transmitter and Receiver devices. Both devices feature a 36-bit “user-friendly” parallel interface with standard logic levels (3.3V CMOS) for easy adaptation to any application.

The link supports an effective (sustained) data rate up to 148.5 MByte/s at the parallel interface, which translates to a serial bit stream of max. 1.188 Gbit/s (payload data rate). With 4 additional bits for link-synchronization, DC-balancing and parity check the maximum bit rate at the serial I/Os is 1.32Gbit/s, for an overall link efficiency of 90 percent. With only 40 ns propagation delay time for both the Transmitter and Receiver, the typical overall latency for a GigaSTaR[®] link is:

$$\text{latency [ns]} = 2 * 40 \text{ ns} + 4\text{ns/m} * \text{cable-length [m]}$$

For example, the latency is about 160 ns for a 20 meter connection with Shielded-Twisted-Pair (STP) copper cable.

1.1 CLOCK SYSTEM

The serial bit clock frequency of 1320 MHz is generated by internal PLLs. The Transmitter and Receiver each require an external 66 MHz reference clock.

A continuous phase alignment in the Receiver ensures that the receive clock is synchronous to the transmit clock.

1.2 PARALLEL DATA FORMAT

Both the GigaSTaR[®] Transmitter and Receiver feature a synchronous 36 bit parallel interface. The maximum frequency at this interface is 33 MHz, equivalent to a period of 30.3 ns for the WRCLK/RDCLK signals.

The PARGEN input pin controls the transfer of the optional external parity bit synchronous with the parallel data. If an external parity bit is provided by the application at the TX_PARITY input pin, PARGEN has to be set to '0'. The Transmitter will read in the external parity bit at the TX_PARITY pin and will compare it with the parity bit generated internally. The TX_PERR# signal reports any mismatch between the external parity bit and the internally generated parity bit.

If no external parity bit is available, PARGEN has to be set to '1' and the Transmitter adds the internally generated parity bit to the data word. The TX_PERR# signal is inactive when PARGEN = '1'.

The Receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal RX_PERR# is asserted for one data cycle. LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

1.3 SERIAL DATA FORMAT

The serial data stream is DC-balanced to support capacitive (AC) coupling for full DC isolation of the link. This is performed by proprietary coding in the Transmitter device.

1.4 TRANSMITTER (TX) CONTROL SIGNALS

TX_RESET# is an asynchronous active low reset signal for the Transmitter device.

TX_PARITY is the input pin for the externally provided parity signal.

TX_PERR = '1' indicates that the externally provided parity bit does not match the internally generated parity bit.

TX_LOCK = '1' indicates that the Transmitter PLL is locked. If TX_LOCK is de-asserted the Transmitter is not ready.

PARGEN = '1' activates the internal parity generation. In this mode, the PARITY input pin is ignored. An internal parity bit is generated and transmitted.

VALID = '1' indicates to the Transmitter that data are available. With the assertion of VALID the RDCLK starts to run. PDATA[35..0] is registered at each rising edge of RDCLK. De-asserting VALID disables RDCLK and stuffing patterns are transmitted over the GigaSTaR® link to maintain synchronization.

A FLAGI positive edge sets an internal flag which is inserted at the end of the data word currently in transmission. The Receiver decodes the flag out of the serial bit-stream and toggles the level of the FLAGO output. This signal can be used to mark the end of a data frame.

1.5 RECEIVER (RX) CONTROL SIGNALS

RX_RESET# is an asynchronous active low reset signal for the Receiver device.

RX_PARITY is the output pin for the parity bit transmitted with the 36 bit data word.

RX_PERR# is asserted for one data cycle if a mismatch of the transmitted and internally generated parity information indicates a transmission failure.

RX_LOCK = '1' indicates that the Receiver PLL is locked. If RX_LOCK is de-asserted, the Receiver is not ready.

EQSEL activates the internal equalizer to support extended cable lengths over 10 meters.

The status bit LSYNC# is asserted if the GigaSTaR® Receiver has successfully synchronized to the incoming bit-stream. If the Receiver is not synchronized correctly, LSYNC# is de-asserted.

RX_PERR# : the receiver permanently computes the parity over each transmitted word and compares it with the transmitted parity bit. A mismatch of both parity information indicates a transmission failure and the signal RX_PERR# is asserted for one data cycle. LSYNC# is de-asserted and the Receiver starts to re-synchronize the link.

The FLAGO output provides the internal flag controlled by the FLAGI input. After a reset, the status of FLAGO is "low".

1.6 LINK MEDIA (COPPER OR FIBER)

The GigaSTaR® Transmitter and Receiver are each equipped with a robust high-speed interface which can be directly connected to impedance-controlled cables (STP or coax), transmission lines or fiber optic modules.

The ING_TRC Piggyback Boards are configured to drive a 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cable with a SUB D9 connector. Initial evaluations with 50 Ohm (100 Ohm differential) Shielded-Twisted-Pair (STP) cables already have proven reliable transmissions at distances of up to 50 meters and beyond (Reference-product: GGSC1608-05/-10/-15/-20/-30/-40/-50, W.L. Gore & Associates). The fiber-optical piggyback board ING_TRF is recommended for longer distances up to 550m.

1.7 TRANSMITTER (TX) SIGNAL TIMINGS

1.7.1 Data Burst Transfers

The data burst timing provides the full data rate of 148.5 MByte/s. VALID is asserted when the first data is valid at PDATA[35..0]. With every rising edge of RDCLK the PDATA inputs are registered, serialized and transmitted. VALID can remain asserted as long as new data are available.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

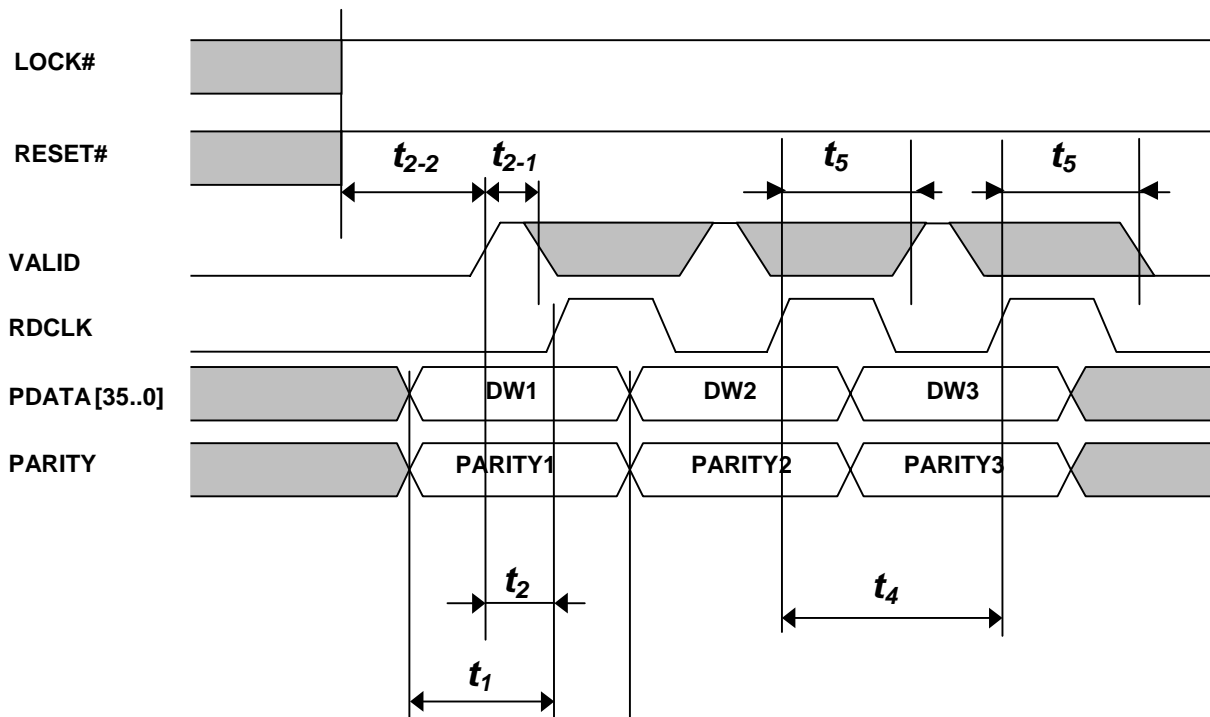


Figure 4: INGT165B Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₁	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t ₂	VALID active to first rising RDCLK edge	9	12	14	ns
t ₂₋₁	VALID high state	5	4		ns
t ₃	PDATA and PARITY hold time	9	6		ns
t ₄	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t ₅	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns
t ₂₋₂	LOCK / RESET high state before Tx operational *	50			μs

Note : For timings with assertion of FLAGI, please see section 3.2.5

*A dislock puls generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 1: INGT165B Data Burst Timing Parameters (under recommended operating conditions)

1.7.2 Single Word Transfers

Single Word Transfers are used to support lower data rates than the maximum parallel data rate of 148.5 MByte/s. VALID has to be de-asserted after the parallel read cycle signaled by one RDCLK pulse. Only one data word is transmitted.

In the timing diagram PARGEN is de-asserted and the application delivers the PARITY bit synchronously to the data word.

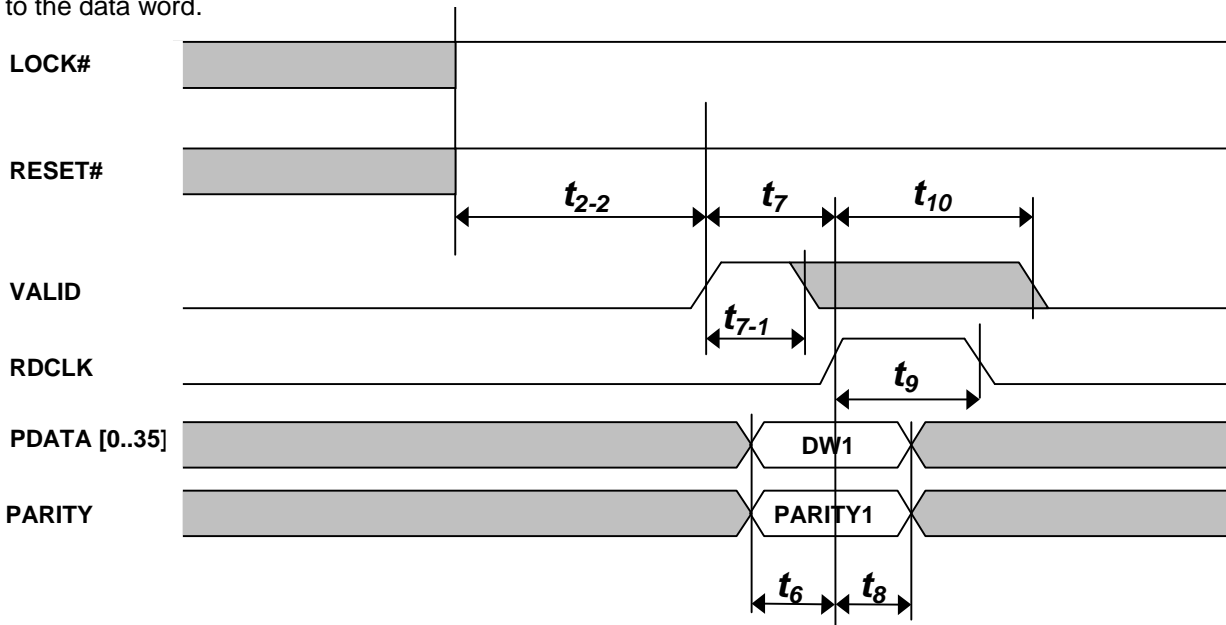


Figure 5: INGT165B Single Word Transfer Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₆	Setup time PDATA and PARITY to RDCLK rising edge	9	6		ns
t ₇	VALID active to rising RDCLK edge	9	12	14	ns
t ₇₋₁	VALID high state	5	4		ns
t ₈	PDATA and PARITY hold time	9	6		ns
t ₉	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t ₁₀	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns
t ₂₋₂	LOCK# / RESET# high state before TX operational *	50			μs

Note : For timings with assertion of FLAGI, please see section 3.2.5

* A dislock puls generates an internal transmitter reset. Therefore both signals have to be at least 50us at high state before transmitter is operational.

Table 2: INGT165B Single Word Transfer Timing Parameters (Under recommended operating conditions)

1.8 RECEIVER (RX) SIGNAL TIMINGS

1.8.1 Data Burst Transfers

The data burst timing is used to support the full data rate of 148.5 MByte/s. RXPDP [35..0] and RX_PARITY are updated with each rising edge of WRCLK (see figure 5).

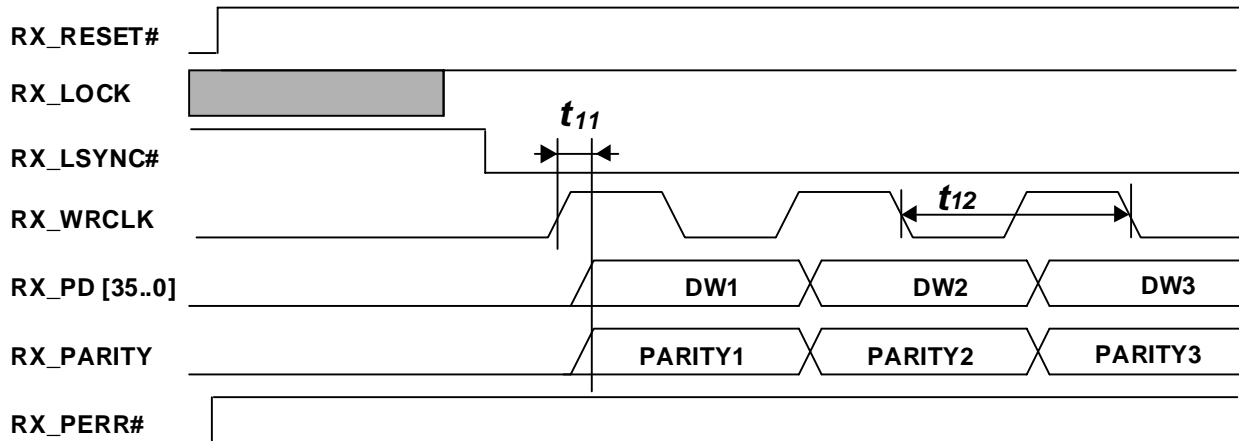


Figure 5: Receiver Data Burst Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t ₁₁	Rising edge WRCLK to RXPd and RX_PARITY bit valid		1	4	ns
t ₁₂	WRCLK cycle time (without assertion of FLAG1)		30.3		ns

Note: For timings with assertion of FLAG1, please see section 1.9

Table 3: Receiver Data Burst Timing Parameters (under recommended operating conditions)

1.8.2 Single Word Transfers

Single Word Transfers are used to support lower data rates. Every time a new data word is received the WRCLK signal generates one clock pulse.

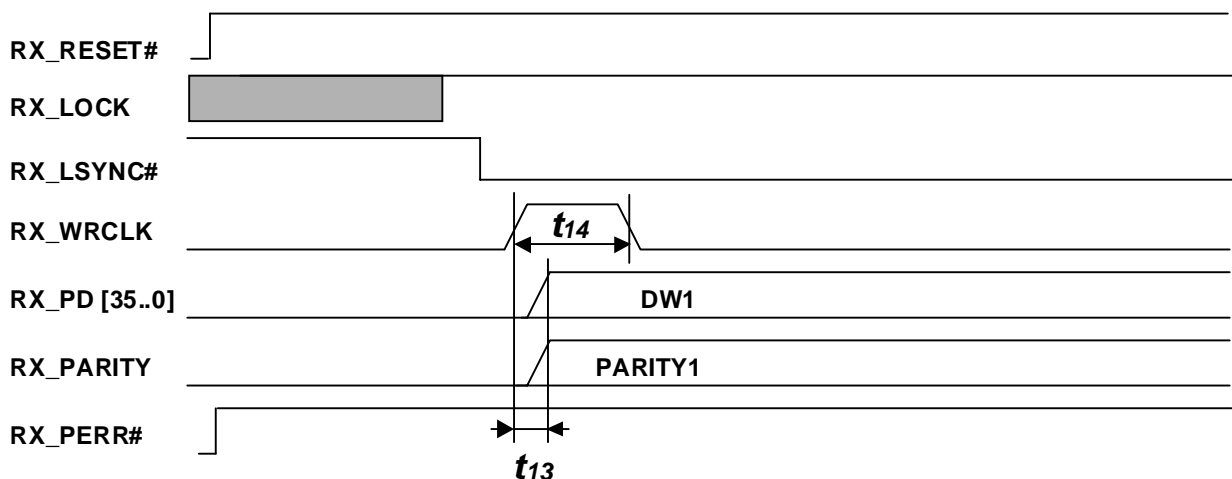


Figure 6: Receiver Single Word Transfer Timing Diagram

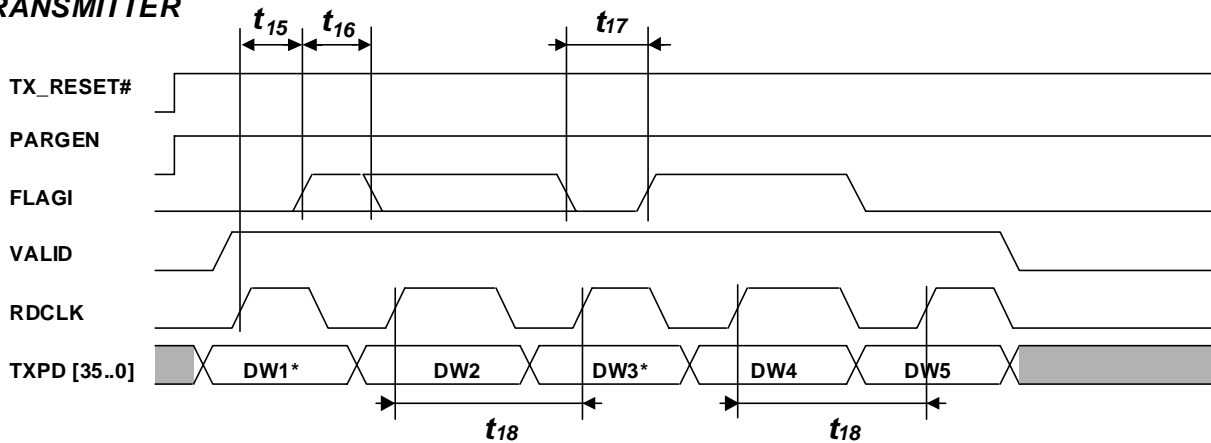
Parameter	Description	Min.	Typ.	Max.	Unit
t ₁₃	Rising edge WRCLK to RXPd and RX_PARITY valid		1	4	ns
t ₁₄	WRCLK high state	14	15	16	ns

Table 4: Receiver Single Word Transfer Timing Parameters (under recommended operating conditions)

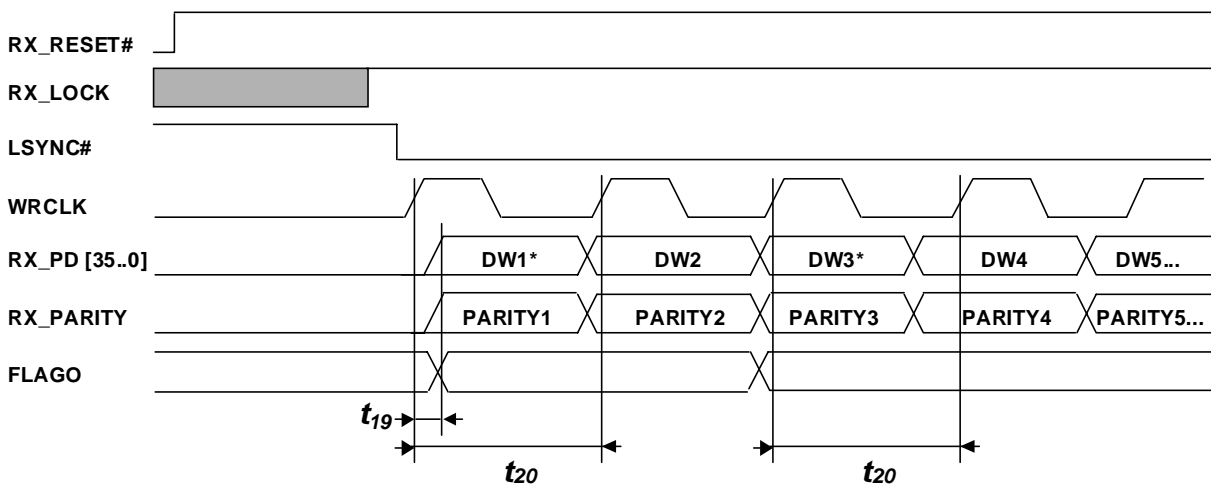
1.9 FLAGI / FLAGO TIMING

With the FLAGI / FLAGO signals a mechanism is provided to implement a side band signalling. Each rising edge at the Transmitter's input FLAGI toggles the FLAGO output of the Receiver. The timing diagram for the FLAGI/FLAGO signal is shown in combination with the Transmitter signals. Note that when the FLAGI signal is asserted, the following RDCLK high state time span is enlarged by app. 6 ns. At the Receiver, the WRCLK low state time span is enlarged by app. 6 ns when the FLAGO output toggles. In the diagrams below, the PARGEN is active at the Transmitter therefore no external parity is provided.

TRANSMITTER



RECEIVER



Note : * indicates the data words [DW1, DW3] that are marked by the FLAGI signal.

Figure 7: INGT165B / INGR165B FLAGI and FLAGO Timing Diagram

Parameter	Description	Min.	Typ.	Max.	Unit
t_{15}	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t_{16}	FLAGI minimum high state		4	6	ns
t_{17}	FLAGI minimum low state		4	6	ns
t_{18}	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t_{19}	Rising edge of WRCLK to RXPD, RX_PARITY and FLAGO valid		1	4	ns
t_{20}	WRCLK cycle time for data word marked by FLAGO toggle		36		ns

Table 5: FLAGI and FLAGO Timing Parameters (under recommended operating conditions)

1.10 ERROR (REPORTING) TIMING

1.10.1 Parity Error (Reporting) Timing

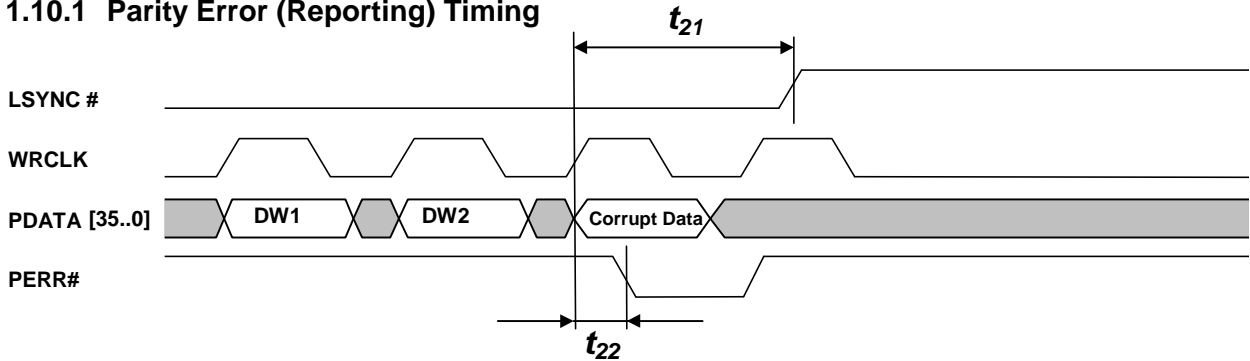


Figure 8: INGR165B Parity Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{21}	Rising edge of WRCLK marking the corrupt data word to rising edge of LSYNC#		1	5	ns
t_{22}	Rising edge of WRCLK marking the corrupt data word to falling edge of PERR#		3	6	ns

Table 6: INGR165B Parity Error (reporting) timing (under recommended operating conditions)

1.10.2 Header/Frame Error (Reporting) Timing

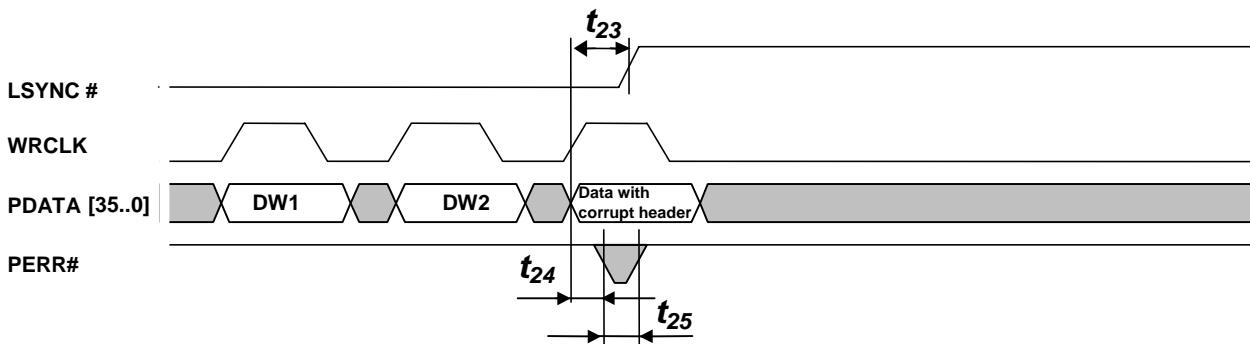


Figure 9: INGR165B Header/Frame Error (reporting) timing

Parameter	Description	Min.	Typ.	Max.	Unit
t_{23}	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0		13	ns
t_{24}	Rising edge of WRCLK marking the corrupt data header to falling edge of PERR#		1,5		ns
t_{25}	PERR # low state		3		ns

Table 7: Header/Frame Error (reporting) timing (under recommended operating conditions)

2. PIGGYBACK BOARD INTERFACE AND MOUNTING DESCRIPTION

2.1 AMP 140 PIN CONNECTOR DEFINITION

Pin (+)	Signal (+)	Pin (-)	Signal (-)	Pin	Signal
4	TXPD0	82	RXPD0	2	GND
6	TXPD1	84	RXPD1	11	GND
8	TXPD2	86	RXPD2	22	GND
10	TXPD3	88	RXPD3	31	GND
14	TXPD4	92	RXPD4	42	GND
16	TXPD5	94	RXPD5	51	GND
18	TXPD6	96	RXPD6	61	GND
20	TXPD7	98	RXPD7	65	GND
13	TXPD8	93	RXPD8	69	GND
15	TXPD9	95	RXPD9	73	GND
17	TXPD10	97	RXPD10	79	GND
25	TXPD11	103	RXPD11	90	GND
19	TXPD12	101	RXPD12	99	GND
24	TXPD13	102	RXPD13	110	GND
26	TXPD14	104	RXPD14	119	GND
28	TXPD15	106	RXPD15	130	GND
30	TXPD16	108	RXPD16	139	GND
27	TXPD17	105	RXPD17	1	VCC
29	TXPD18	107	RXPD18	12	VCC
34	TXPD19	112	RXPD19	21	VCC
33	TXPD20	111	RXPD20	32	VCC
36	TXPD21	114	RXPD21	41	VCC
37	TXPD22	115	RXPD22	52	VCC
38	TXPD23	116	RXPD23	62	VCC
35	TXPD24	113	RXPD24	80	VCC
39	TXPD25	117	RXPD25	89	VCC
40	TXPD26	118	RXPD26	100	VCC
44	TXPD27	122	RXPD27	109	VCC
45	TXPD28	123	RXPD28	120	VCC
54	TXPD29	132	RXPD29	129	VCC
48	TXPD30	126	RXPD30	140	VCC
53	TXPD31	131	RXPD31	23	Reserved, set to GND (*)
47	TXPD32	125	RXPD32	63	Reserved, set to VCC (*)
56	TXPD33	134	RXPD33	67	Reserved, do not connect (*)
49	TXPD34	127	RXPD34	71	Reserved, do not connect (*)
55	TXPD35	133	RXPD35	57, 59, 60	Not connected
7	TX_LOCK	87	RX_LOCK	64, 66, 68	Not connected
9	TX_PARITY	91	RX_PARITY	70, 72, 74	Not connected
58	TX_PERR#	136	RX_PERR#	75, 76, 77	Not connected
3	TX_RESET#	81	RX_RESET#	78, 124	Not connected
5	RDCLK	83	WRCLK	135, 137	Not connected
43	FLAGI	121	FLAGO	138	Not connected
46	PARGEN	85	EQSEL		
50	VALID	128	LSYNC#		(*) : These pins are reserved for optional functions

Table 8: Piggyback AMP 140 Pin Free Height Connector Pin Definition (AMP #179029-6)

By choosing an AMP free height receptacle among AMP part numbers AMP177983-6/AMP5-179009-6/AMP 5-179010-6, the spacing between the Piggyback Board and the main board can be selected to be 6, 10 or 14 mm.

The pin numbering definition of the AMP connector is shown in Fig. 10:

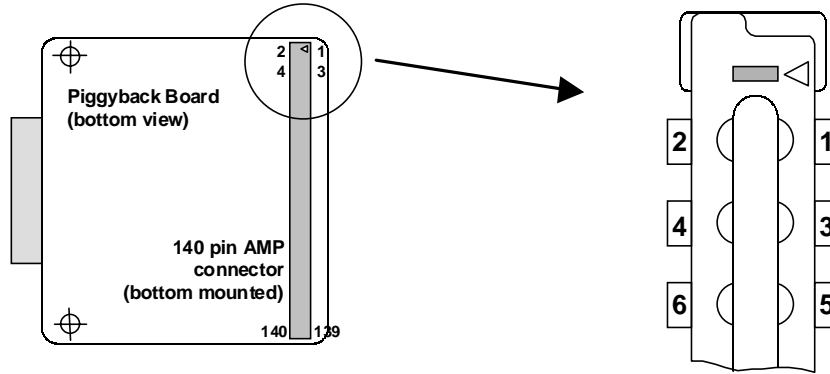


Fig. 10: Piggyback AMP 140 pin connector numbering

2.2 SERIAL TRANSMISSION CABLE TERMINATION

The SUB D9 cable connector plugs directly into the transmission reference cables (GGSC1608-05/-10/-15/-20/-25/-30-50, W.L. Gore & Associates). Besides the AC coupling capacitors providing 50 V DC isolation per line end, a dedicated cable termination is mounted on the bottom side of the piggyback board to the SUB D9 connector pins. The default delivery termination is matched for the GGSC1608-10 (10 meter Gore GigaSTaR[®] cable). As the inductance value of this termination is a function of the transmission cable characteristic, the termination has to be matched to the cable if another cable than GGSC1608-10 is used:

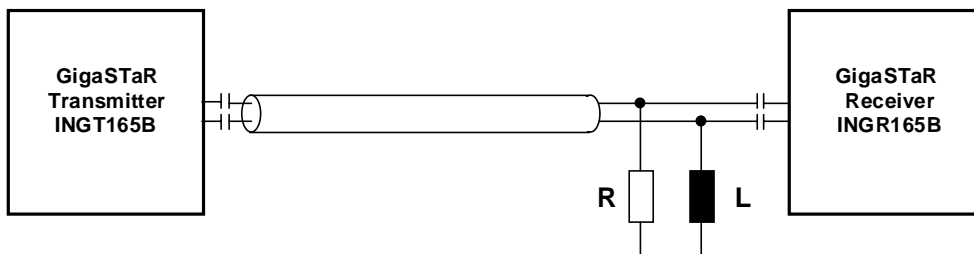


Figure 11: Piggyback cable termination scheme

Gore cable type number	Cable length	R value (SMD type 0805)	L value (SMD type 1210)
GGSC1608-05	5 meter	100 Ohm	22 nH
GGSC1608-10 (delivery configuration)	10 meter	100 Ohm	47 nH
GGSC1608-20	20 meter	100 Ohm	220 nH
GGSC1608-30	30 meter	150 Ohm	220 nH

Table 9: Various Gore GGSC1608 cable lengths with corresponding termination values

Note : For other cable lengths or cable types than shown in table 9, other termination values may apply, please call your distributor support line for further information.
For a Piggyback Board connected e.g. to a GGSC1608-5 cable with a loopback connector, the termination value for the GGSC1608-10 cable applies.

The termination devices are mounted on the bottom side of the SUB D9 connector, on the solder flags as shown in Figure 12. This figure also shows the front view pinout of the SUB D9 connector:

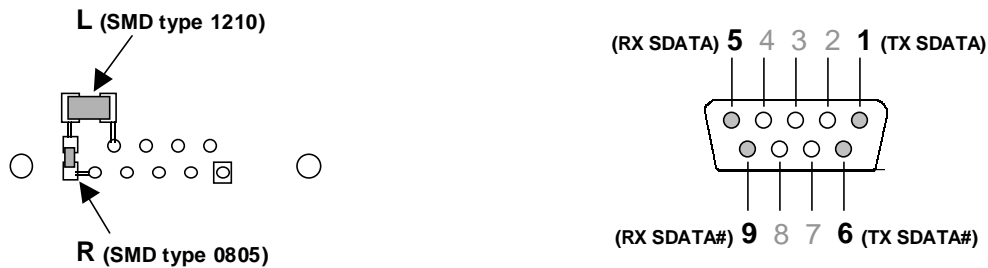


Figure 12: Serial transmission cable termination components and SUB D9 connector front view pinout

3. PIGGYBACK BOARD SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings define values beyond which damage to the device may occur. Inova Semiconductors may not be held liable for any product degradation or damage caused by a violation of the absolute maximum ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above those indicated in the recommended operating conditions is not guaranteed.

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	-0.5	+4.2	V	
Input Voltage	V_{IN}	-0.5	$V_{CC}+0.5$	V	
I/O Current (DC or transient any pin)	I_D	-20	+20	mA	
Ambient Temperature (under bias)	T_B	-40	+70	° C	
Storage Temperature	T_{stg}	-40	+85	° C	
Static Discharge Voltage (AMP connector pins)	V_{SDAMP}		± 2000	V	Human Body Model
Static Discharge Voltage (DB9 connector pins)	V_{SDDB9}		± 800	V	Human Body Model

Table 10: Absolute Maximum Ratings

3.2 RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Units	Note
DC Supply Voltage	V_{CC}	+3.15	+3.45	V	
Input Voltage	V_{IN}	0	V_{CC}	V	$V_{CC} = 3.3V \pm 0.15V$
Ambient Temperature	T_a	-40	+70	° C	Air flow ≥ 250 LFPM

Table 11: Recommended Operating Conditions

3.3 ELECTRICAL SPECIFICATION

3.3.1 DC – Characteristics (under recommended operating conditions)

Parameter	Symb ol	Test Condition	Min.	Typ.	Max.	Unit
Input High Voltage	V _{IH}		2.6			V
Input Low Voltage	V _{IL}				0.7	V
Input High Current	I _{IH}	V _{IN} = V _{CC}	-10		10	μA
Input Low Current	I _{IL}	V _{IN} = 0 V	-10		-150	μA
Output High Voltage	V _{OH}	I _{OH} = -0.5 mA	0,95 V _{CC}			V
Output Low Voltage	V _{OL}	I _{OL} = 1.5 mA			0,05 V _{CC}	V
LOCK Output High Current	V _{LH}	I _{OH} = -0.5 mA	0,9 V _{CC}			mA
LOCK Output Low Current	V _{LL}	I _{OL} = 1.5 mA			0,1 V _{CC}	mA
Supply Current	I _{CC}	Max. data transmission rate		600	800	mA
Power Dissipation	P _D	Max. data transmission rate		2,0	2,8	W

Table 12: DC – Characteristics (under recommended operating conditions)

3.3.2 AC- Characteristics (under recommended operating conditions)

Parameter	Description	Min.	Typ.	Max.	Unit
t ₁	Setup time TXPD and TX_PARITY to RDCLK rising edge	9	6		ns
t ₂	VALID active to first rising RDCLK edge	9	12	14	ns
t ₂₋₁	VALID high state	5	4		ns
t ₂₋₂	LOCK# / RESET# high state before Tx operational	50			μs
t ₃	TXPD and TX_PARITY hold time	9	6		ns
t ₄	RDCLK cycle time (without assertion of FLAGI)		30.3		ns
t ₅	Rising RDCLK edge to sampling window for VALID state (VALID=0: exit BURST mode, VALID=1: continue BURST mode)	18	20	22	ns
t ₆	Setup time TXPD and TX_PARITY to RDCLK rising edge	9	6		ns
t ₇	VALID active to rising RDCLK edge	9	12	14	ns
t ₇₋₁	VALID high state	5	4		ns
t ₇₋₂	LOCK# / RESET# high state before Tx operational	50			μs
t ₈	TXPD and TX_PARITY hold time	9	6		ns
t ₉	RDCLK high state (without assertion of FLAGI)	14	15	16	ns
t ₁₀	Rising RDCLK edge to sampling window for VALID state (VALID=0: continue single word mode, VALID=1: enter BURST mode)	18	20	22	ns
t ₁₁	Rising edge WRCLK to RXPd and RX_PARITY bit valid		1	4	ns
t ₁₂	WRCLK cycle time (without assertion of FLAGI)		30.3		ns
t ₁₃	Rising edge WRCLK to RXPd and RX_PARITY valid		1	4	ns
t ₁₄	WRCLK high state	14	15	16	ns
t ₁₅	Rising edge of RDCLK to rising edge of FLAGI	0		18	ns
t ₁₆	FLAGI minimum high state		4	6	ns
t ₁₇	FLAGI minimum low state		4	6	ns
t ₁₈	RDCLK cycle time after assertion of FLAGI (one cycle only)		36		ns
t ₁₉	Rising edge of WRCLK to RXPd, RX_PARITY and FLAGI valid		1	4	ns
t ₂₀	WRCLK cycle time for data word marked by FLAGO toggle		36		ns
t ₂₁	Rising edge of WRCLK after the corrupt data word to rising edge of LSYNC#		1	5	ns
t ₂₂	Rising edge of WRCLK marking the corrupt data word to falling edge of RX_PERR#		3	6	ns
t ₂₃	Rising edge of WRCLK marking the corrupt data header to rising edge of LSYNC#	0		13	ns
t ₂₄	Rising edge of WRCLK marking the corrupt data header to falling edge of RX_PERR#		1,5		ns
t ₂₅	RX_PERR # low state		3		ns

Table 13: AC - Characteristics (under recommended operating conditions)

3.4 PIGGYBACK BOARD DIMENSIONS

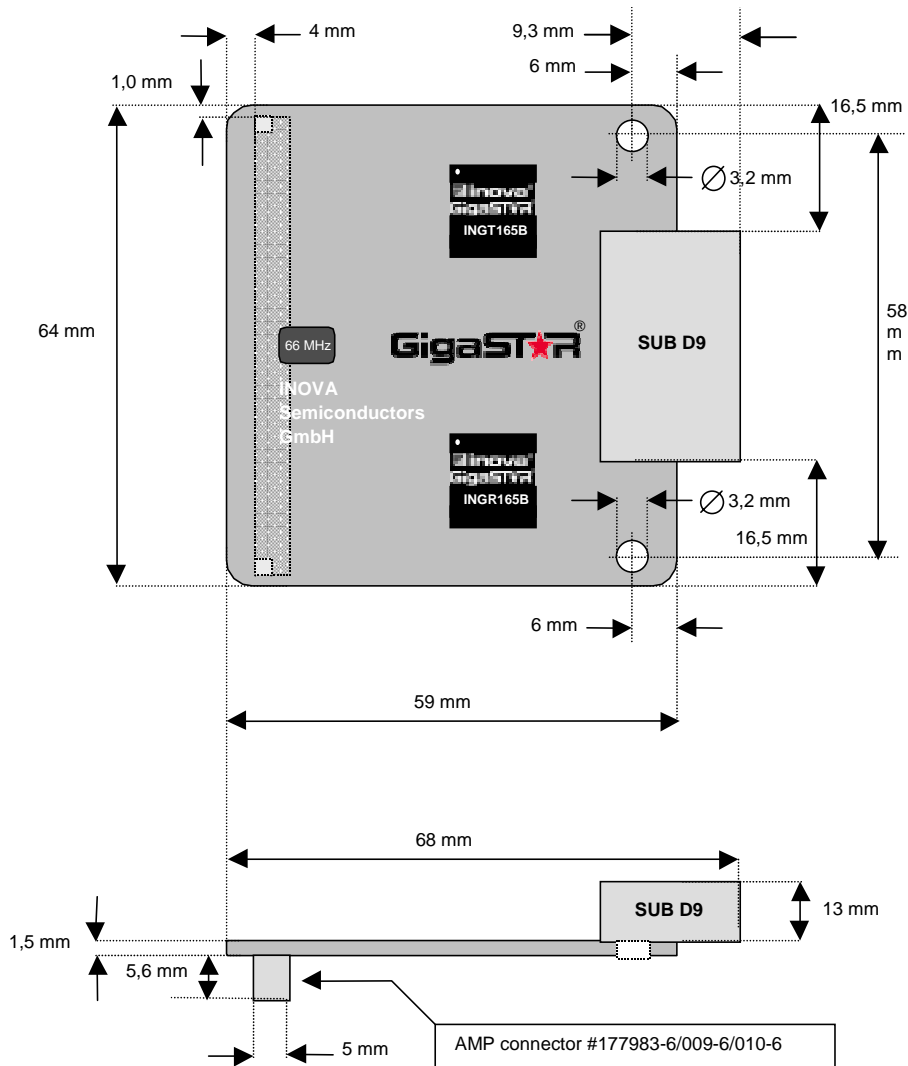


Figure 13: Top and side view of the ING_TRC Piggyback Board with mechanical outlines

3.5 HANDLING PRECAUTIONS

Handling precautions are:

1. The maximum ratings may not be exceeded at any time.
2. Precautions have to be taken against exposure of the board terminals to electrostatic discharge stress.
3. Mounting and dismounting of the AMP connector and receptacles have to be performed with care.
4. The mounting/dismounting cycles should be limited in order to avoid AMP connector wearout.
5. For ambient temperatures exceeding 50°C, an air flow of ≥ 250 LFPM should be provided.
6. The piggyback board is not EME-shielded and must not be operated in an environment where its electromagnetic emissions can cause malfunctions of other boards or devices.


3.6 ORDERING CODE AND PRODUCTION STATUS INFORMATION

Ordering Code	Delivery option	Production Status
ING_TRC	Piggyback full duplex Board configured for the 10 m Gore GGSC1608-10 cable	full production

Table 14: Product Availability

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