

# AN 100 Automotive Usage

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## APIX – Video Interface configuration

### Abstract

APIX (Automotive **PIX**el Link) is a high speed serial link for transferring Video/Audio data in Cameras and Displays in Automotive Applications such as Infotainment and Driver Assistance systems. The link supports a downstream data rate of up to 1 Gbit/s. In addition, APIX features a full duplex, bidirectional sideband channel over the same or a separate link. This link can be used to implement an independent control channel.

This application note describes in detail the configuration of the video interface of the INAP125T12/24 APIX transmitter and INAP125R12/24 APIX receiver devices.

### System Architecture

The APIX Interface devices provide an uni-directional parallel TTL video interface and a bi-directional sideband interface (Figure 1). The serial interconnection between transmitter and receiver device comprises a high speed differential down link and if required a lower speed differential up link.

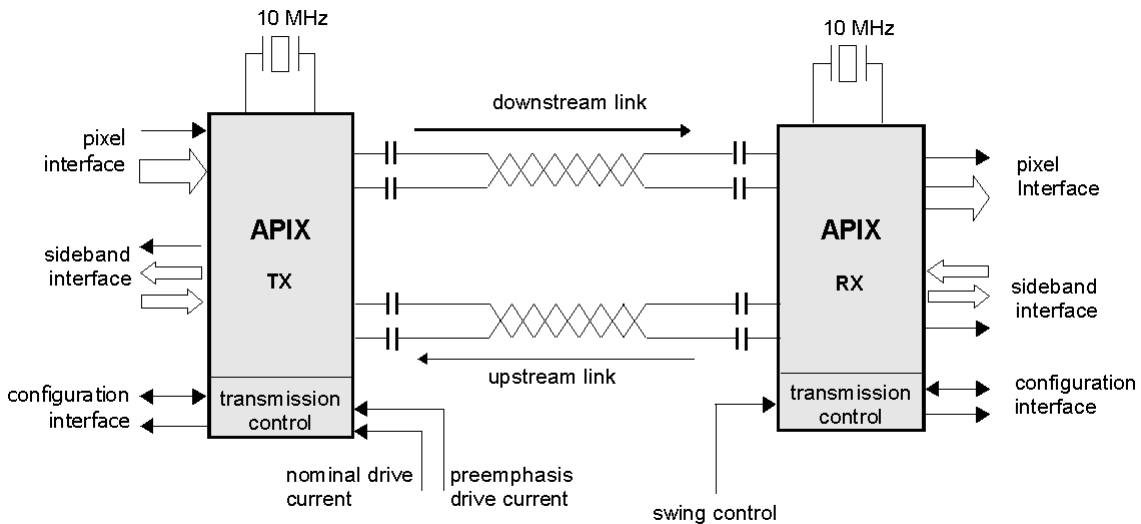


Figure 1: APIX parallel and serial interconnections

Alternatively the upstream link can also be established via common mode signaling on the down link twisted pair. This allows an implementation of the entire link with only two wires, however impacting the EMI robustness of link, since the upstream sideband data is transferred as common mode signal.

For automotive applications it is recommended to use the dedicated CML data link in upstream direction.

## 1.0 Video interface overview

The APIX link is designed for the direct connection of high resolution TFT displays and CMOS image sensors to central graphic and image processors, offering high speed transmission over a long distance with low EMI. The parallel video interface of the APIX devices can be configured individually to match all popular display and image sensor interfaces.

The link acts as transparent gateway for the parallel interface, in the following also called video or pixel interface, providing the data sampled at the interface at the transmitter at the same clock at the receiver. Due to this transparent characteristics, the interface may not only be used for video data, it allows the transport of any data sampled at the interface pins.

The APIX video interface supports parallel RGB format with four different bit widths of 10,12,18 or 24 bit. In addition to the pixel data interfaces, three pixel control signals are implemented on the video interface. The video interface provides a pixel clock with programmable active edge (rising/falling) and programmable control signal polarity. The pixel interface width at the transmitter and receiver has to be identical, to provide the correct function of the pixel interface.

The Video Data Interface operates in parallel to the Side-Band Data Interfaces, which offer downstream and upstream capabilities (see [2]).

The APIX high speed link operates independently of the pixel data speed or format. The video transport can be seen as kind of conveyor belt, which is continuously filled with data frames. The belt has a constant speed of 500MBit/s or 1GBit/s. The frames include video data, downstream sideband data and balancing overhead. In case of lower pixel clock rates, the frames are filled with „dummy“ data, which are ignored at the receiver.

Figure 1-2 illustrates the general conveyor belt functionality of the high speed data stream, including the overhead and sideband data.

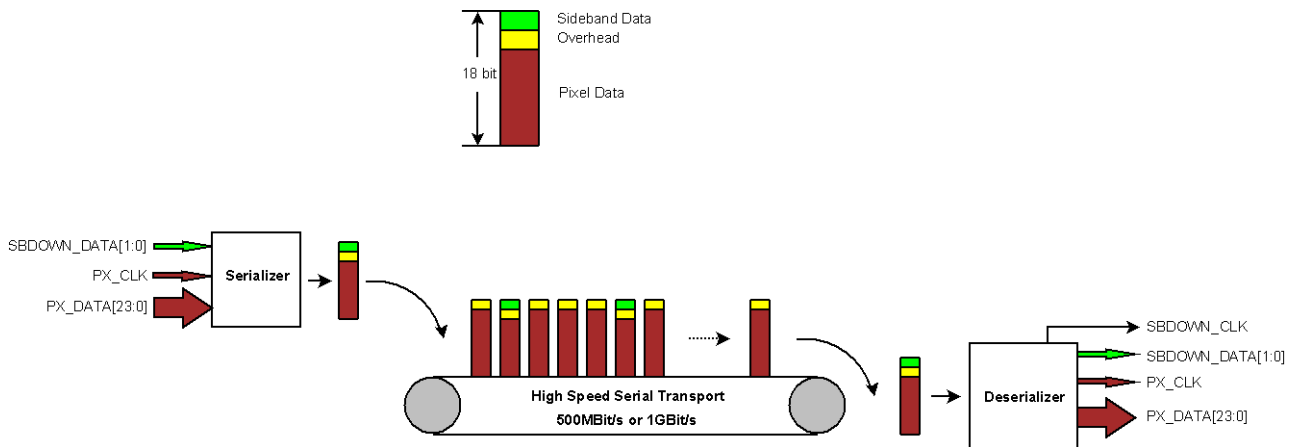


Figure 1-2: APIX High Speed transport stream

## 2.0 APIX Clock Domains

The APIX technology features a fundamental advantage to pixel clock driven devices by implementing a dedicated clock system for the high speed serial link. With this, the serial link is not influenced by any variances or jitter at the pixel clock which lowers the risk for EMI issues. In addition, the link offers „hot-plug“ capabilities, as the high speed link synchronizes immediately on power up or connect and independently to video data.

The APIX transmitter features two separate clock domains for the video stream, which decouples the pixel clock of the link clock driving the high speed serial line. Video data consisting of parallel pixel data for color information and pixel control data for the framing of the image are registered in a video data buffer. The data buffer performs the clock domain crossing of the pixel clock domain and the system clock domain.

At the receiver, the link clock is recovered from the serial data stream and serves as reference for the main system clock. The recovered data are deframed and decoded and pushed into the receiver video data buffer. Finally, these data are provided at the pixel data interface, synchronous to the also recovered pixel clock. The following chapters discuss the different domains in more detail.

Please see Figure 2-3 for an overview of the different clock domains in the complete APIX video data path.

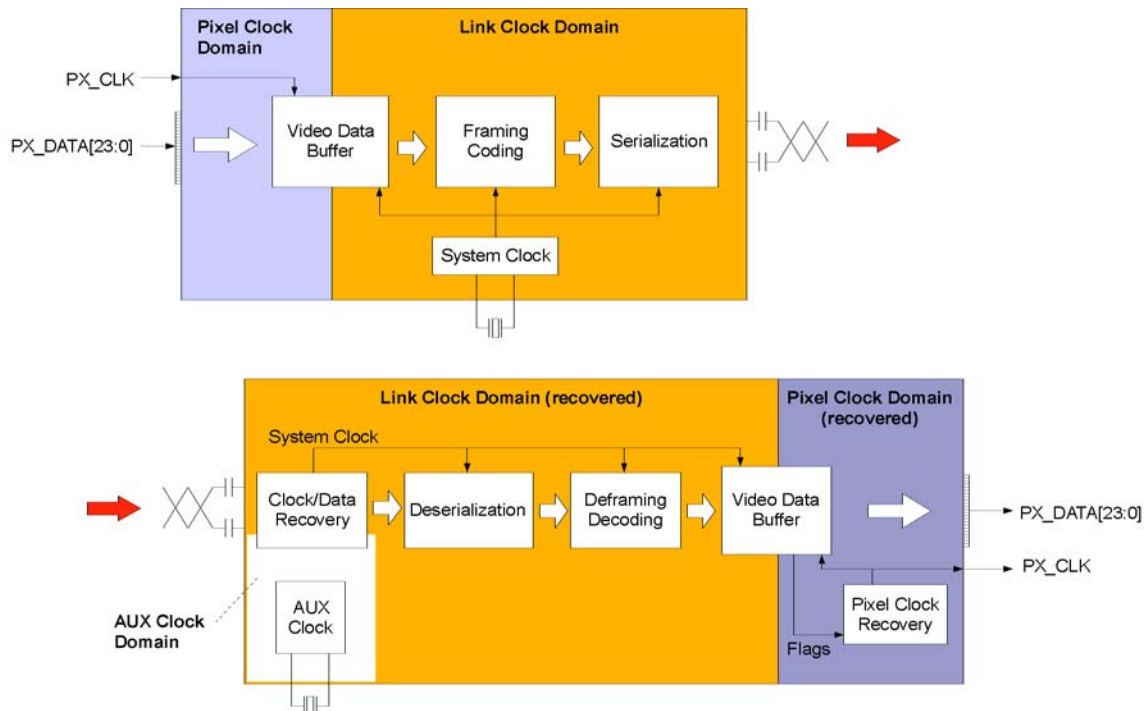


Figure 2-3: Video Data path through APIX link

## 2.1 Pixel Clock Domain

The pixel clock at the transmitter needs to be provided by the main controller or graphics controller. Depending on the configuration of the transmitter interface (see [1]), the pixel data are sampled at the rising or the falling edge of the clock. The pixel data are sampled into a video data buffer and read out by the framing unit, which runs at the internal system clock. Therefore the video buffer acts as decoupling unit between the external pixel clock and the internal system clock.

The decoupling of the link clock and the pixel clock has several advantages. It facilitates the implementation of multiple pixel data interfaces and guarantees a pixel clock independent link bandwidth which is the prerequisite for an efficient implementation of generic sideband data channels. Any variances or jitter do not affect the high speed serial link. It is moreover the basis for high performance and a low bit error rate of the physical layer.

The pixel clock recovery unit at the receiver generates a pixel clock which, depending on the buffer status, dynamically adapts the clock output. This dynamic handling avoids buffer under or overruns and also acts as de-jitter function for variances occurring at the pixel clock input at the transmitter. Please see Section 5.0 for a detailed description of the de-jitter function.

## 2.2 Link Clock Domain

The APIX link clock is derived from the transmitter system clock which is based on the external crystal. At the transmitter, the system clock drives the framing and coding units and is used to sample the video data from the video buffer. The system clock acts as basis for the high speed PLL, which generates the 500MHz or 1GHz clock for the serializer. Since the high speed clock is independent of the pixel clock, the signal quality of the high speed link is not affected by variances at the video interface.

The clock and data recovery unit (CDR) at the receiver regenerates the system clock, derived from the serial data stream. The system clock serves as main clock for the deframing and decoding of the data frames and is used to push the data into the video data buffer.

## 2.3 AUX Clock domain (RX only)

The receiver devices need to be supplied with an external crystal circuit, which is used to generate the AUX clock domain. This clock only serves as reference for the CDR to recover data and system clock from the high speed serial link.

## 3.0 Video interface configuration

The video interface of the APIX devices consists of the following data pins:

- PX\_DATA[23:0]
- PX\_CTRL[2:0]
- PX\_CLK

It is recommended to consider series resistors for all PX\_DATA, PX\_CTRL and PX\_CLK input pins close to the video source device to reduce the risk of data-related emissions and reflections.

### 3.1 Data width

The PX\_DATA interface samples the parallel RGB data and can be configured to be driven in 10bit, 12bit, 18bit or 24bit mode. The configuration has to be stored as device configuration vector at address 02, bits [1:0] and gets active after reset.

Pixel control data like HSYNC, VSYNC and DATA ENABLE have to be connected to the PX\_CTRL interface (please see Section 3.3).

Configuration setting of address 02, bits [1:0]

- 00: 10bit
- 01: 12bit
- 02: 18bit
- 03: 24bit

In case of a data with smaller than 24, it is recommended to pull the remaining pins to GND, e.g. for 18bit interface pins PX\_DATA[23:17].

### 3.2 Pixel clock active edge

Pixel data are sampled (TX) or provided (RX) at pins PX\_DATA[23:0] at either rising or falling edge of Pixel clock (PX\_CLK). The selection of the falling or rising edge is done by the configuration vector.

Configuration setting of address 2, bit 5

- 0: falling edge
- 1: rising edge

The sampling edge is a local setting only and does not affect the remote device. For example, it is possible to sample in PX\_DATA with rising edge at TX and eject the same data on the Rx side with falling edge and vice versa.

### 3.3 Pixel Control PX\_CTRL

The PX\_CTRL[2:0] signals are dedicated pins to carry the video control signals HSYNC, VSYNC and DATA ENABLE. The pins are sampled at PX\_CLK and transmitted transparently to the receiver. However, DATA ENABLE is also used by the APIX devices to align the data stream and to recognize the start of the pixel data.

- PX\_CTRL0: HSYNC
- PX\_CTRL1: VSYNC
- PX\_CTRL2: DATA ENABLE

The DATA ENABLE (DE) signal is mandatory for correct operation of the APIX link. DE needs to be enabled for a minimum of 4 pixel clocks for correct operation.

#### 3.3.1 Transmitter

At the transmitter, a rising edge of DE indicates the start of a new set of data. In order to realign the data to the frame structure at the serial link, the serializer uses a new empty frame at the serial link. The active frame is filled with „empty“ data. The APIX devices offer different operation modes (see Section 3.4) to configure the density of the DE signal for video streaming.

Figure 3-4 illustrates the segmentation of the pixel data to the 16 bit frame structure with the example of 18 bit data width and shows the impact of DE on the frame alignment of the transmitter. The example shows the transmission of 4 Pixels. Pixel 0 is sent together with a rising edge at DE and therefore forces a realignment at the serial link.

The figure is simplified as it doesn't consider different payload sizes of the frames for sideband data.

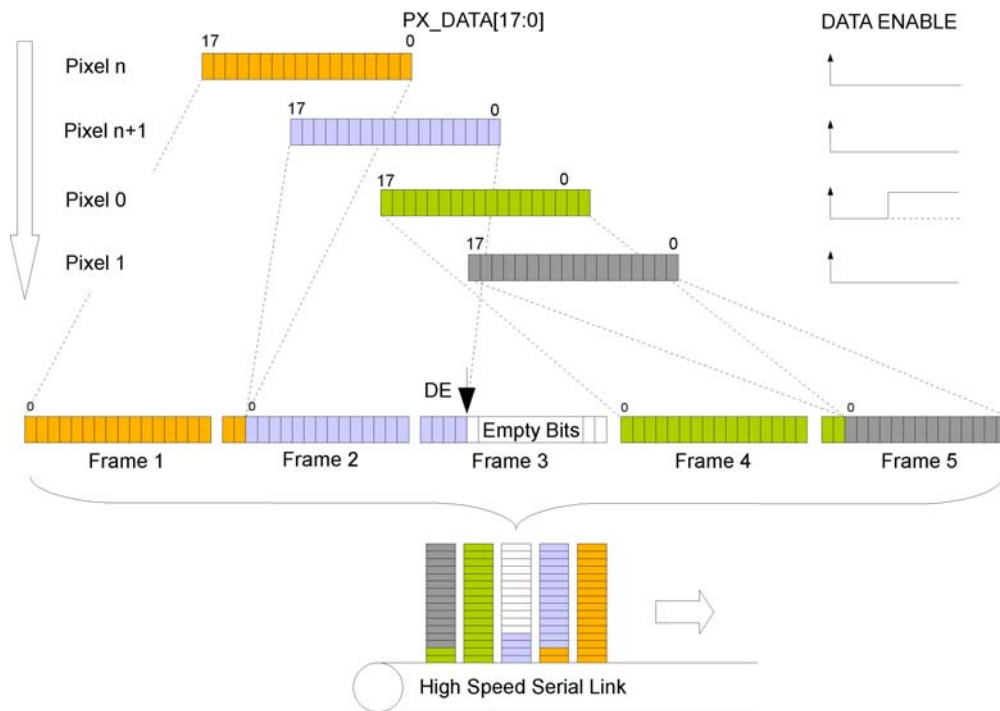


Figure 3-4: Segmentation of pixel data and alignment to DATA ENABLE

### 3.3.2 Receiver

The DATA ENABLE (DE) signal sampled at the transmitter is used by the receiver to synchronize to the correct frame alignment. With DE, the receiver recognizes the start of a set of pixel data and is able to align the received bits to the pixel interface. This is especially important at the initial start of data transmission after power-up or connect. Therefore it is mandatory to send DE at least once at the beginning of the transmission to align the receiver pixel data output to the serial stream. During normal transmission DE ensures the correct re-alignment in case of transmission errors.

### 3.4 Pixel control operation modes

There are three different operation modes how to transmit the PX\_CTRL signals which are configurable by the dedicated bits of the Tx device configuration vectors.

Configuration setting of address 2, bits [3:2]

- 00: PX\_CTRL signals will never be transmitted
- 01: (reserved)
- 10: PX\_CTRL signals will be transmitted on every second (even) pixel
- 11: PX\_CTRL signals will be transmitted on each pixel

When using the PX\_CTRL signals the bandwidth will be reduced because the 3 control signals are appended to the pixel data (10, 12, 18 or 24 pixel bits + 3 control bits). Please see Section 4.0 for the impact on the maximum bandwidth available with the different settings.

NOTE: DATA ENABLE (PX\_CTRL2) needs to be provided regardless of the configuration of the PX\_CTRL signals. Even if the setting is set to 'never transmit' the signal is required by the devices to align the pixel data.

### 3.5 Upper left corner configuration

When using APIX in a display application, some TFT screens require to have a defined start of the display data. The APIX receiver features to initialize to the upper left corner of the display that is adjusted by the PX\_CTRL signals HSYNC, VSYNC and DATA ENABLE. The configuration is done using the following settings:

Configuration setting of address 3, bit 1

- 0: no adjustment
- 1: PX\_DATA and PX\_CTRL start at the upper left corner

Configuration setting of address 3, bit 2

- 0: no adjustment
- 1: PX\_CLK starts at the upper left corner

### 3.6 Pixel clock PX\_CLK

The pixel clock PX\_CLK input (TX) or output (RX) defines the synchronous clock used at PX\_DATA and PX\_CTRL. The maximum pixel clock is limited by the bus width used at PX\_DATA and the mode, PX\_CTRL data are sent over the link. Please refer to Section 4.0 on page 8 for the maximum bandwidth available for each mode.

The pixel clock output at the receiver is recovered from the incoming data stream and the result of a VCO control loop with external loopfilter. A control logic monitors the status of the video buffer and generates the PWM signal used to control the VCO through the external loopfilter. With this, the VCO generates a pixel clock which keeps the buffer status in a controlled range. Please see Table 3-1 for recommended values for the loopfilter design.

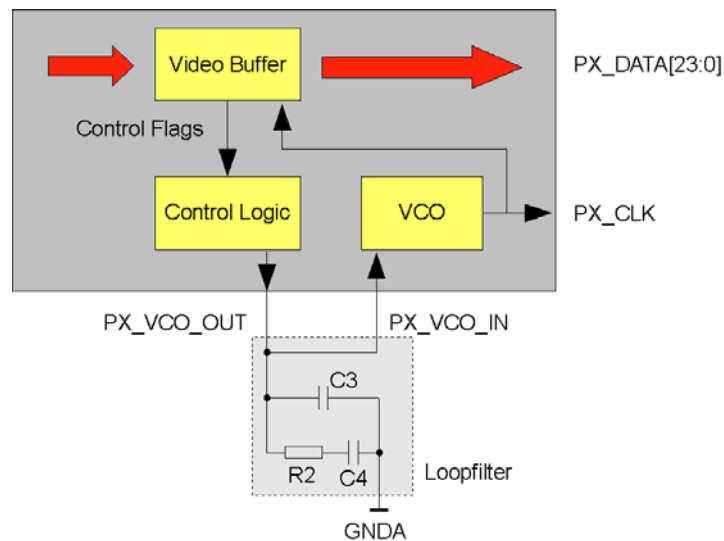


Figure 3-5: Pixel Clock recovery control loop

Parameter	Symbol	Value	Units
Loop Filter Capacitor C3	C3	2.2	nF
Loop Filter Capacitor C4	C4	47	nF
Loop Filter Resistor R2	R2	1	kΩ

Table 3-1: Recommended Loop Filter values for the Pixel Clock Recovery

The status of the video buffer has impact on the PWM signal to the loopfilter and therefore to the output frequency of the VCO. If the buffer indicates „nearly full“, the loop reduces the VCO frequency and therefore the speed, the buffer is read out with. On „nearly full“, the frequency is increased respectively. Please see Figure 3-6 for a simplified diagramm for the pixel clock control.

The loop generates a pixel clock, which on average reflects the pixel clock sampled at the transmitter. Jitter and variances at the transmitter pixel clock are reduced or even filtered, depending on their deviation and modulation. Please see Section 5.0 for more details on this topic.

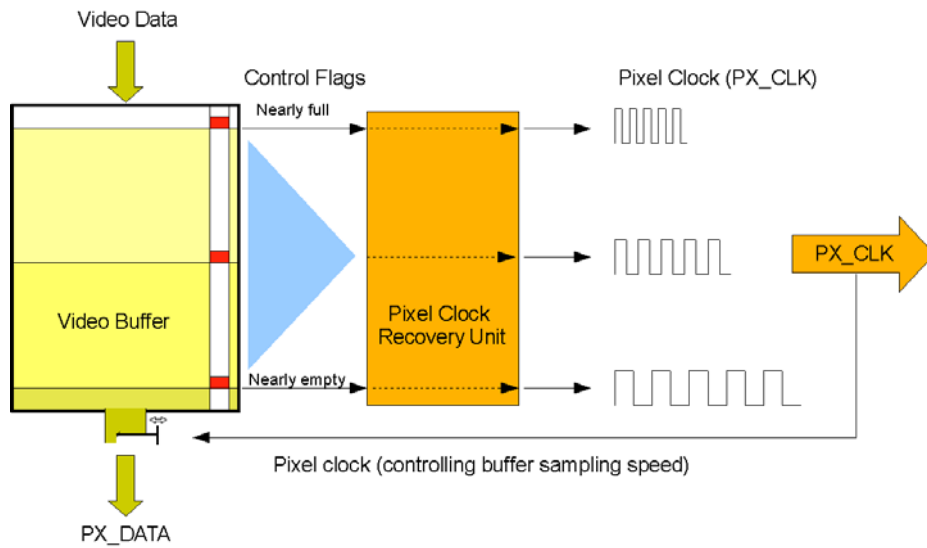


Figure 3-6: Pixel clock control by video buffer status

## 4.0 Transmission Bandwidth

The high speed serial link of the APIX link can be configured to operate at either 1 GBit/s full bandwidth mode or at 500 MBit/s half bandwidth mode. The transmission bandwidth for the video data is defined by the pixel clock, the configuration of the width of the pixel data interface and the amount of control data (PX\_CTRL) sent with the data. The pixel clock shall not exceed the values as defined in Table 4-2.

Parameter	Min	Typ.	Max.	Unit
Pixel Clock Frequency	6		62	MHz

Table 4-2: Pixel Clock range specification

The different configuration result in the theoretical maximum pixel clock frequencies, as shown in Table 4-3.

Channels	PX_DATA Width	control signal transmit mode configuration of transmission of pixel control signals		
		never	even pixels only	each pixel
Downstream Bandwidth 1GBit/s net bandwidth 847MBit/s	10 bit	62.0 MHz <sup>a</sup>	62.0 MHz <sup>a</sup>	62.0 MHz <sup>a</sup>
	12 bit	62.0 MHz <sup>a</sup>	62.0 MHz <sup>a</sup>	56.5 MHz
	18 bit	47.1 MHz	43.4 MHz	40.3 MHz
	24 bit	35.3 MHz	33.2 MHz	31.4 MHz

Table 4-3: Maximum pixel clock frequency for different PX\_CTRL and data width settings

Channels	PX_DATA Width	control signal transmit mode configuration of transmission of pixel control signals		
		never	even pixels only	each pixel
Downstream				
Bandwidth 500MBit/s net bandwidth 423,5	10 bit	42.4 MHz	36.8 MHz	32.6 MHz
	12 bit	35.3 MHz	31.4 MHz	28.2 MHz
	18 bit	23.5 MHz	21.7 MHz	20.2 MHz
	24 bit	17.6 MHz	16.6 MHz	15.7 MHz

**Table 4-3: Maximum pixel clock frequency for different PX\_CTRL and data width settings**

a. Due to the internal VCO, the pixel clock is limited to 62 Mhz as specified in Table 4-2.

The transmission bandwidth and the pixel clock define the maximum video resolution possible with the APIX link. The maximum video resolution depends on the color depth (10,12,18 or 24 bit), the number of control bits (always, even or never), the link bandwidth (500 or 1000 Mbit/s) and the refresh for the video stream.

Table 4-4 and Table 4-5 show possible configurations for different displays with the required refresh rate of 60Hz. Please note that the calculations are based on the requirements for VESA compliant displays requiring additional information for HSync, VSync and blanking timing. Therefore the „real“ resolution bandwidth is larger than the ones listed below.

Name	Resolution	Color depth (Bit)	PX_CTRL transmission
QVGA	320x240	24	each pixel
VGA	640x480	24	each pixel
WVGA	854x480	24	even pixels only
WVGA	854x480	18	each pixel
SVGA	800x600	18	each pixel
XGA	1024x768	12	never
XGA	1024x768	10	each pixel

**Table 4-4: VESA video resolution settings at 1 GBit/s, Refresh rate 60Hz (Examples)**

Name	Resolution	Color depth (Bit)	PX_CTRL transmission
QVGA	320x240	24	each pixel
VGA	640x480	12	each pixel

**Table 4-5: VESA video resolution settings at 500 MBit/s, Refresh Rate 60Hz (Examples)**

Name	Resolution	Color depth (Bit)	PX_CTRL transmission
WVGA	854x480	12	never
WVGA	854x480	10	each pixel
SVGA	800x600	10	never

Table 4-5: VESA video resolution settings at 500 MBit/s, Refresh Rate 60Hz (Examples)

## 5.0 Pixel clock jitter

As indicated in Section 3.6, the pixel clock at the transmitter is decoupled from the serial link. Therefore, jitter or variances at this clock do not affect the high speed serial link. The pixel clock recovery at the receiver extracts the clock from the data stream and adjusts it according to the video buffer status. Assuming an ideal pixel clock with no jitter and noise, the pixel clock output at the receiver has the same frequency as on the transmitter input.

Besides the fact that a jitterless pixel clock is not realistic due to EMI, component and design constraints, variances may be even advantageous in terms of EMI as they spread the emitted spectrum of the clock and therefore may lower the emissions.

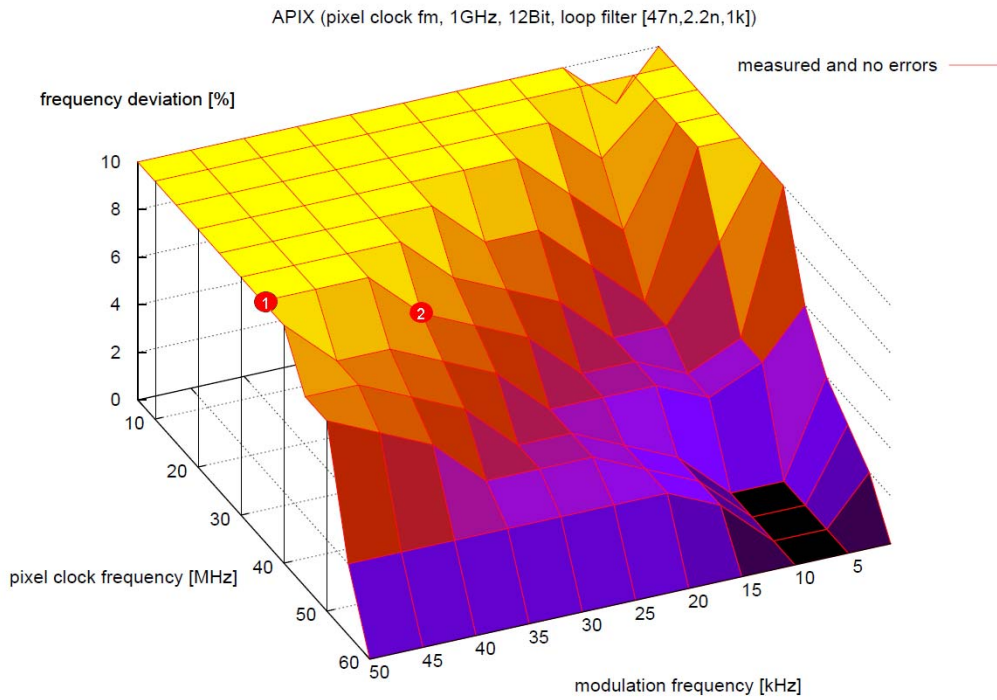
Even though, the APIX link itself is not impacted, the jitter may cause data errors depending on the deviation and modulation of the variance.

The path from pixel clock input to pixel clock output can be seen as PLL, generating a specific frequency and stabilizing by the control loop. The PLL base frequency would be the nominal pixel clock frequency (e.g. 20Mhz). Jitter would appear as frequency drift (deviation, e.g. short drift to 20.5Mhz) and the frequency of the occurrence (modulation, e.g. 1Khz).

In order to identify the dependency of the pixel clock output frequency from the jitter, the data error rate at the link has been measured in reference to pixel clocks at different bit width, frequency, jitter modulation and deviation. The results are displayed as 3D graph for each bit width.

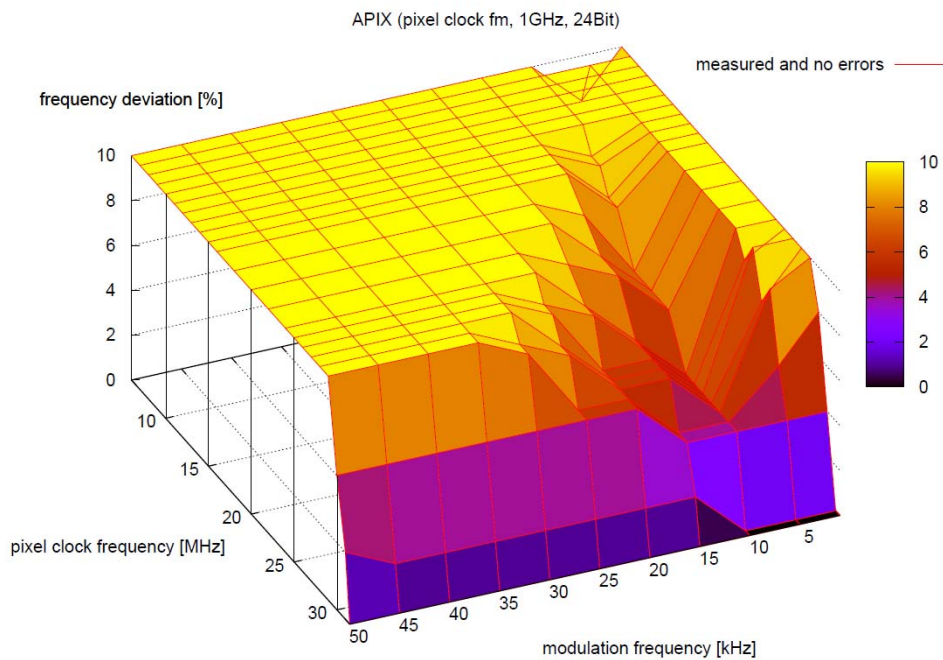
Figure 5-7 shows the example of a 12bit interface at 1Gbit/s bandwidth mode. The tests were performed in a way that on each test, the transmitter pixel interface was supplied with a specific pixel clock and a deviation at a specific modulation. E.g. the tests started at 6Mhz pixel clock frequency, with a deviation of 2% (0.12Mhz) at 1kHz. In case no data errors were detected on the link, the deviation was increased to 4% and so on. The deviation was measured up to 10%, the modulation was swept between 1 and 50kHz.

Looking at the graph, the yellow area indicates the configurations, on which no errors occurred with the deviation of 10%. The result shows that the maximum possible deviation in general increases with increasing the modulation frequency. For example, at a pixel clock of 35Mhz, no errors occurred with 50khz modulation and 10% (3.5MHz) deviation (highlighted as point 1). The modulation frequency could be reduced to 35khz until errors occurred, maximum deviation possible therefore reduced to 8% (highlighted as point 2).



**Figure 5-7: Dependency of data error rate of pixel clock deviation and modulation with 12bit interface**

Figure 5-8 shows the relationship of error rate versus frequency deviation and modulation with the 24bit interface.



**Figure 5-8: Dependency of data error rate of pixel clock deviation and modulation with 24bit interface**

## Bibliography

- [1] – DS\_INAP125T and DS\_INAP125R, Datasheets, Inova Semiconductors GmbH
- [2] – AN 101, Using the Sideband channels, Application Note, Inova Semiconductors GmbH

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