

AN101 Automotive Usage

Order ID: AN_INAP_101
 February 2009
 Revision 1.3

APIX – Using the Sideband channels

Abstract

APIX (Automotive **PIX**el Link) is a high speed serial link for transferring Video/Audio data in Cameras and Displays in Automotive Applications such as Infotainment and Driver Assistance systems. The link supports a downstream data rate of up to 1 Gbit/s. In addition, APIX features a full duplex, bidirectional sideband channel over the same or a separate link. This link can be used to implement an independent control channel.

This application note describes in detail how to connect and configure the INAP125T to use the sideband interface.

System Architecture

The APIX Interface devices provide an uni-directional parallel TTL video interface and a bi-directional sideband interface (Figure 1). The serial interconnection between transmitter and receiver device comprises a high speed differential down link and if required a lower speed differential up link.

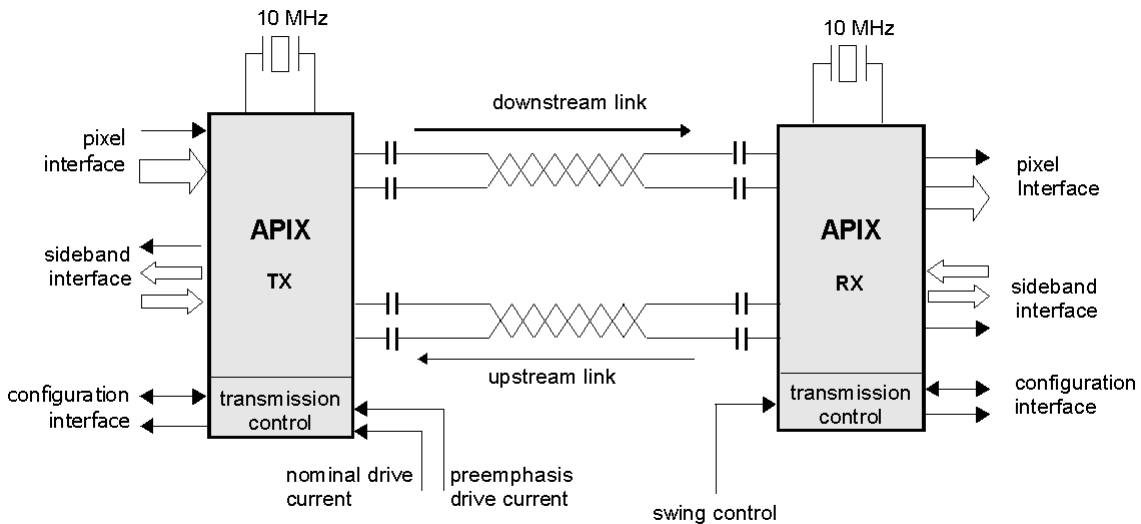


Figure 1: APIX parallel and serial interconnections

Alternatively the upstream link can also be established via common mode signaling on the down link twisted pair. This allows an implementation of the entire link with only two wires, however impacting the EMI robustness of link, since the upstream sideband data is transferred as common mode signal.

For automotive applications it is recommended to use the dedicated CML data link in upstream direction.

Introduction to the Side band Interface

Common Serializer / Deserializer (SERDES) devices are designed and optimized to convert parallel data into a high speed serial stream, which is transmitted from a TX device to a RX device using differential signalling. This serial transmission allows higher speed and longer range with the benefit of very low EMI over a single pair of cables. However, the link is optimized for uni-directional high speed data as required in video streaming applications.

Especially in automotive applications, the requirements for higher integration and reuse of existing media gets more and more important. Besides video data, systems like Rear Seat entertainments or remote cameras require power supply and control data to be exchanged with the main unit with a minimum amount of cables.

To address these requirements, the APIX technology features up to 2 full duplex, bidirectional sideband channels on the same or a separate pair of cables. This link offers full flexibility from the transmission of simple status flags, directly sampling interfaces like UART or SPI, up to complex protocols like AShell (see [2]). The AC coupled physical layer allows to induce the DC power supply for the remote system like cameras onto the APIX data lines.

Compared to other SERDES implementations, APIX offers the advantage to be able to send sideband data independent to the video interface. The video interface clock often is used as main reference clock for transmitter and the high speed serial link. This architecture forces the pixel clock to be active for sending sideband data or to keep the link alive. This gets especially critical for applications requiring upstream capabilities with random data like keyboard or remote control.

Within the APIX devices the high speed serial link is „decoupled“ from the video data interface by using a separate system clock for the serial link (see [3]). The link powers up and synchronizes independently to the pixel clock, therefore there's no need for special video interface handling to drive the sideband.

The APIX architecture supports full duplex operation by implementing the upstream sideband channel either embedded as common mode signaling or on a dedicated cable.

Sideband interface

The sideband interface on both the transmitter and receiver devices consists of the data pins and the corresponding clock outputs. The sideband data inputs are sampled asynchronously to the application using an internally generated reference clock and are transmitted with low latency. At the sideband data outputs the data are provided in sync to the sampling clock.

For the APIX link, the downstream sideband channel is defined as serial stream from the transmitter to the receiver, the upstream sideband channel as serial stream from receiver to the transmitter.

The Sideband data are available or have to be supplied to the following pins

- SBDOWN_DATA[1:0]¹:
 - Data input (TX) or data output (RX) of the downstream data
- SBDOWN_CLK:
 - Clock output at RX, synchronous clock for SBDOWN_DATA
- SBUP_DATA[1:0]¹:
 - Data output (TX) or data input (RX) of the upstream data
- SBUP_CLK:
 - Clock output at TX, synchronous clock for SBUP_DATA

Please see also Figure 2 and Figure 3 for the sideband data flow in both directions.

1. The number of available data pins depends on the package. Please check [1] for available package options.

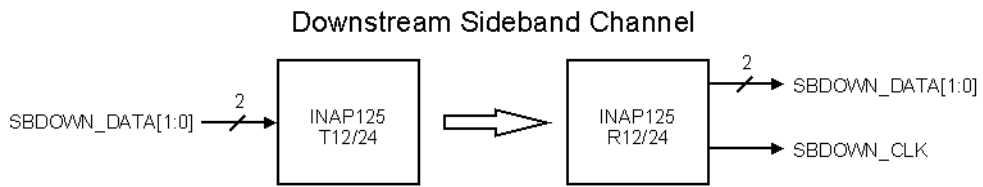


Figure 2: Downstream sideband channel pins

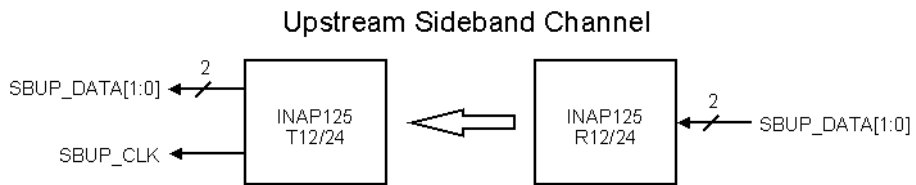


Figure 3: Upstream sideband channel pins

Downstream and upstream link have different clocking and sampling schemes, which are described in the following sections.

Downstream

In order to support both video and separate sideband channel, the downstream data path is a combination of the data sampled at the pixel data interface PX_DATA[23:0] and the sideband data SBDOWN_DATA[1:0]. The transmission is performed as merged frames of 18bits, which typically hold 16 bits of data and 2 bits of balancing overhead. The sideband bits are filled in every 4th frame, which guarantees a constant bandwidth.

Figure 4 illustrates the merged transport of sideband and pixel data on the downstream.

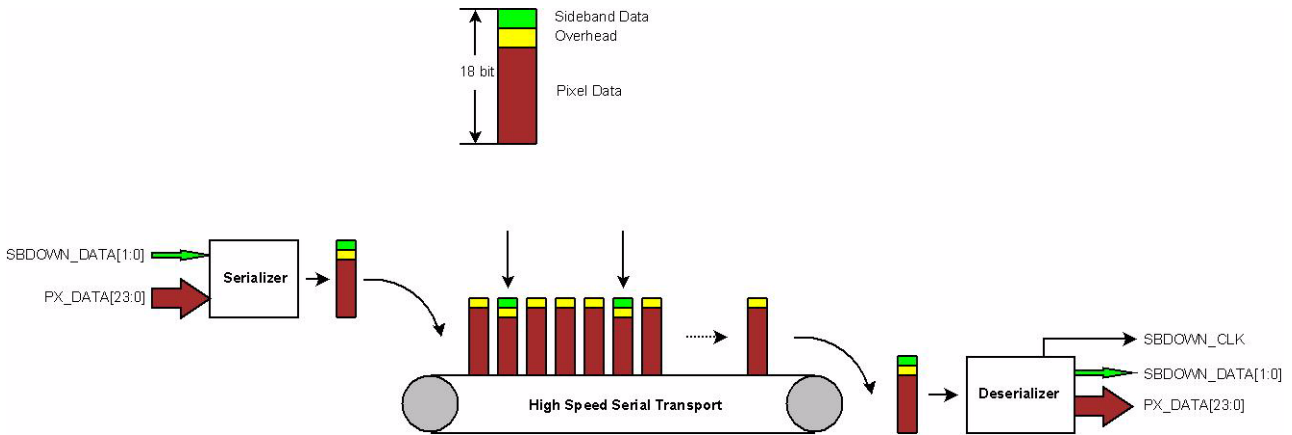


Figure 4: Downstream transport including sideband data (simplified)

The maximum gross downstream data rate for the APIX link is 1Gbit/s. Considering the values for payload and overhead, the sampling rate for the downstream sideband pins at 1Gbit/s can be calculated to

$$1\text{GHz} / (4 * 18) = 13.89 \text{ MHz}$$

for 500Mbit/s mode this results in

$$500\text{MHz} / (4 * 18) = 6.94 \text{ MHz}$$

This sampling clock is derived as divided clock from the internal system clock at the transmitter devices INAP125Txx. As the sideband interface is sampled asynchronously, the maximum bandwidth for a digital data stream is slightly lower than the sampling frequency.

Please see Table 1 as summary of the sampling frequency in the different bandwidth modes. The downstream speed is configured by a configuration vector (see [1]).

Downstream speed	SBDOWN_DATA[1:0] Sampling frequency
1Gbit/s	13.89 MHz
500 MBit/s	6.94 MHz

Table 1: Downstream Sideband bandwidth and sampling frequency

The receiver clock data recovery (CDR) at the receiver devices extracts the clock and data and provides them at SBDOWN_CLK and SBDOWN_DATA[1:0].

Downstream Jitter and Latency

Due to the asynchronous sampling of the SBDOWN_DATA pins, the data output at the receiver includes a certain jitter compared to the data sampled at the transmitter. The maximum jitter is defined by the time between two rising edges of the sampling clock and therefore mainly defined by the sampling frequency. Figure 5 illustrates overall latency between the sampled and received data at SBDOWN_DATA as combination of the jitter and the transmission delay.

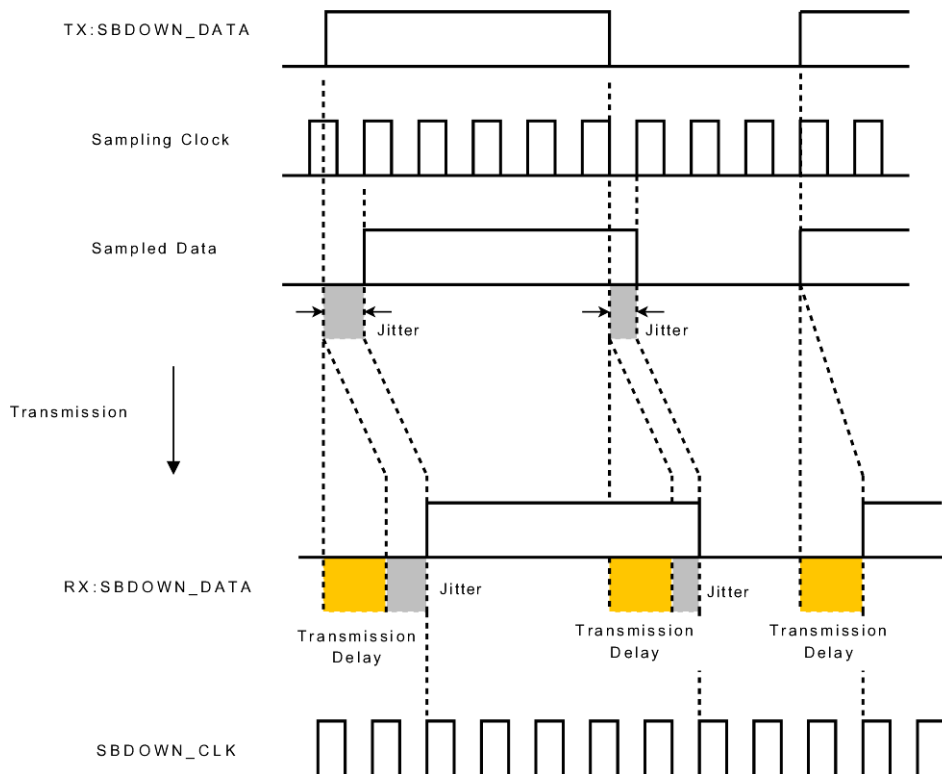


Figure 5: Jitter and transmission delay of the sideband transmission

The transmission delay results from the transmission line, which depends on the cable length and the processing time of the chip.

The following plots at Figure 6 and Figure 7 show SBDOWN_DATA at the receiver compared to SBDOWN_DATA input at the transmitter at a cable length of 1 meter and 5 meter. As illustrated in Figure 5, the transmission delay grows with the cable length, while the jitter stays at a constant rate of about 72ns, which reflects the 13.89MHz sampling frequency. In 500Mbit/s mode, the jitter increases to 144ns as the system clock and the sampling frequency is halved to 6.94MHz. The overall latency increases accordingly.

Please note, that the values below have to be seen as examples and can vary between different cables and chips. The measurements have been performed using the standard APIX evaluation kit and Leoni Dacar 538 cables.

Channel 2: TX SBDOWN_DATA Input
Channel 3: RX SBDOWN_DATA Output

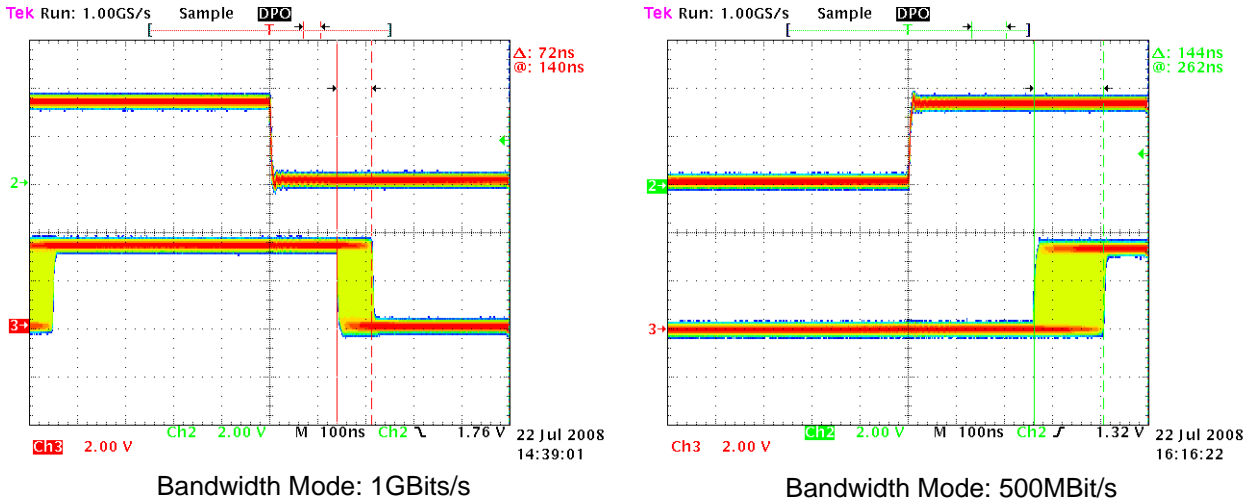


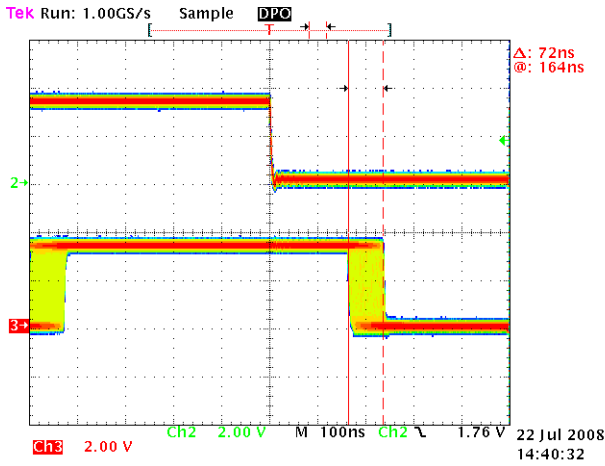
Figure 6: Transmission Delay and Jitter at a cable length of 1m

Please see Table 2 for an overview of maximum jitter and latency of the downstream sideband link at 1m cable length.

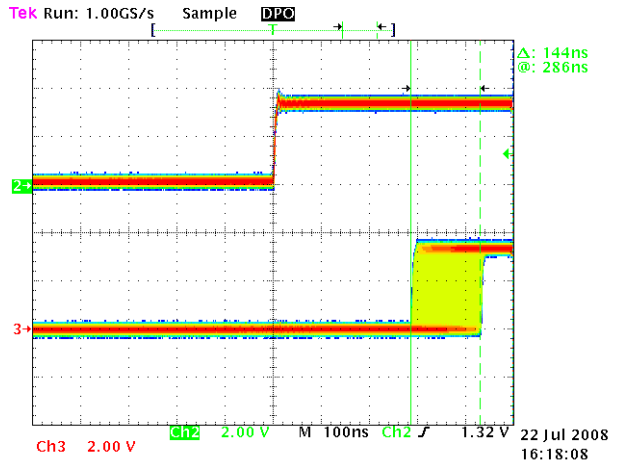
Bandwidth mode	Maximum jitter	Downstream delay @ 1m (measured)	Maximum Latency
1 GBit/s	72 ns	140 ns	212 ns
500 MBit/s	144 ns	264 ns	408 ns

Table 2: Downstream jitter and latency at a cable length of 1m

Channel 2: TX SBDOWN_DATA Input
Channel 3: RX SBDOWN_DATA Output



Bandwidth Mode: 1GBit/s



Bandwidth Mode: 500MBit/s

Figure 7: Transmission Delay and Jitter at a cable length of 5m

Bandwidth mode	Maximum jitter	Downstream delay @ 5m (measured)	Maximum Latency
1 GBit/s	72 ns	164 ns	236 ns
500 MBit/s	144 ns	286 ns	430 ns

Table 3: Downstream jitter and latency at a cable length of 5m

Upstream

The APIX link features a flexible upstream link, which is established either

- embedded, via common mode signaling, using the same pair of cables as the downstream.
- dedicated, via differential signaling, using a separate pair of cables.

Both signaling modes do not require any switching mechanism at the driver stage of the differential signals, which may cause switching noise and therefore EMI issues. In addition, both modes allow full duplex operation of upstream and downstream.

However, common mode signaling uses the shield of the cable for the back-current. Therefore the benefit of using a single pair of cables may not be applicable for the stringent EMI requirements of automotive applications. Using the dedicated upstream functionality would be recommended for these applications.

Upstream data are sampled and provided at SBUP_DATA[1:0]. Similar to the downstream sideband, the pins are sampled asynchronously by an internally generated clock. The upstream data stream is handled independently to the downstream speed, which provides higher flexibility on sampling frequency and bandwidth.

The upstream data are sent in frames of 3 bit, consisting of 2 bits of data and 1 bit overhead. The upstream serial clock can be configured to a maximum value of 62.5 MHz, which leads to a maximum bit clock per channel of

$$(62.5 \text{ MHz} / 3 \text{ bit}) / 2 \text{ channels} = 10.41 \text{ MHz}$$

The selection for the transmission mode and the sampling frequency needs to be performed as parameter in the configuration vector (see [1]). The upstream link requires the configuration to be done at both the transmitter and the receiver devices. The main bandwidth mode configuration defines the general system clock, thus also influences the upstream sampling frequency.

Please see Table 4 as summary for all different configurations possible for the upstream link.

Configuration	Configuration Options
Dedicated upstream	Enable / Disable
Embedded upstream	Enable / Disable
Bandwidth Mode	1 GBit/s / 500 MBit/s
Upstream Link serial clock 1GBit/s^a	Upstream serial clock / Sampling freq. 62.5 MHz / 10.41 MHz 41.7 MHz / 6.94 MHz 31.25 MHz / 5.21 MHz
Upstream Link serial clock 500 MBit/s^a	Upstream serial clock / Sampling freq. 62.5 MHz / 10.41 MHz 31.25 MHz / 5.21 MHz 20.83 MHz / 3.47 MHz

Table 4: Upstream configuration

a. defined by bandwidth mode configuration

Upstream data and clock are provided at the transmitter at SBUP_DATA[1:0] and SBUP_CLK.

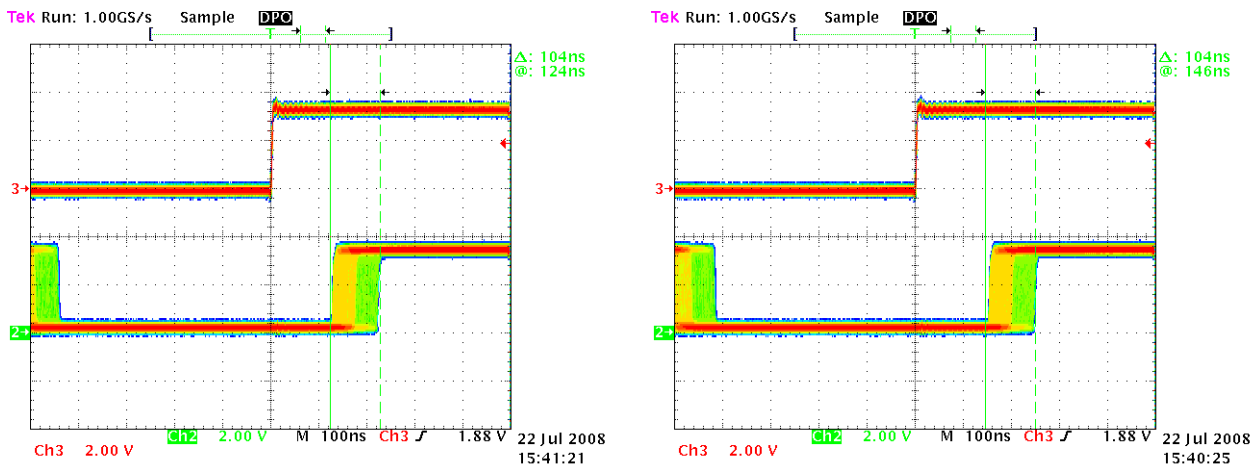
Upstream Jitter and Latency

Similar to the downstream link, the upstream sideband transmission link introduces a certain latency and jitter onto the data path. The upstream data path can be configured to different sampling speeds and settings. Since the upstream uses its own sampling and framing scheme, the transmission latency and jitter are not affected by the bandwidth mode selection (1Gbit/s, 500Mbit/s) directly. However, it is affected by the sampling frequency, which is defined by the upstream serial line clock setting.

Figure 8 shows the influence of the cable length on the upstream sideband.

Channel 3: RX SBUP_DATA Input
Channel 2: TX SBUP_DATA Output

Sampling frequency: 62.5MHz



Cable Length: 1 meter

Cable Length: 5 meter

Figure 8: Upstream Transmission Delay and Jitter

The maximum upstream jitter again depends on the sample frequency and is specified as listed in Table 5.

Upstream serial line clock	Sample frequency	Maximum jitter
62.50 MHz	10.41 MHz	104 ns
41.67 MHz	6.94 MHz	152 ns
31.25 MHz	5.21 MHz	200 ns
20.83 MHz	3.47 MHz	304 ns

Table 5: Maximum upstream jitter for the different serial line clocks

Table 6 and Table 7 show the latency calculated from the jitter and the measurements at the test board. The measurements have shown a transmission delay of the cable of approximately 5.5 ns per meter for this setup.

Upstream serial line clock	Maximum jitter	Transmission Delay measured @ 1m	Maximum Latency
62.50 MHz	104 ns	134 ns	238 ns
31.25 MHz	200 ns	304 ns	504 ns
20.83 MHz	304 ns	432 ns	706 ns

Table 6: Upstream Latency at 500Mbit/s

Upstream serial line clock	Maximum jitter	Transmission Delay measured @ 1m	Maximum Latency
62.50 MHz	104 ns	126 ns	230 ns
41.67 MHz	152 ns	230 ns	382 ns
31.25 MHz	200 ns	292 ns	492 ns

Table 7: Upstream Latency at 1Gbit/s

Bibliography

- [1] – INAP125T and INAP125R Datasheets, Digital Automotive Pixel Link Datasheets, Inova Semiconductors
- [2] – AShell Technical Documentation, Inova Semiconductors
- [3] – AN 100, Video Interface Configuration Application Note, Inova Semiconductors

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