

## GigaSTaR<sup>®</sup> – Bit Error Rates

This application note provides information on the Bit Error Rate (BER) of the GigaSTaR link. It is commonly known that the BER of a data transmission system is impossible to simulate or calculate due to the contributing factors of all system components (IC, connectors, cables, etc.). The approach used in this application note is statistical methods, known from reliability and failure rate calculations, to the BER. A bit error is considered herein, as a failure of a component. The data used to provide evidence of the device hours tested is derived from production testing of over 500 board-level products ING\_TRC, ING\_TTC/RRC and ING\_TRF.

The calculations result in a failure rate per hour, which is then used to calculate the failure rate per second, and per bit, providing the Bit Error Rate.

Documented device hours during board production tests:

$$t_T = 500 * 8 * 1000 \text{ seconds} = 4 \text{ E6 s} = 1111 \text{ device hours; Failures} = 0$$

Chi-Square distribution function value for 90% CL, 0 Failures:

$$\chi^2 = 4.605$$

$$\text{Failure rate: } \lambda = \frac{\chi^2}{2 * t_T} = \frac{4.605}{2 * 1111 \text{ h}} = 2.1 / 1000 \text{ h} = 0.6 * 10^{-6} / \text{s}$$

As the GigaSTaR operates permanently with a total data rate of 1.32 Gbit/s, the BER calculates as:

$$\text{BER}_{(90\%CL)} = \frac{\lambda}{1.32 * 10^9 \text{ bit / s}} = \frac{0.6 * 10^{-6} / \text{s}}{1.32 * 10^9 \text{ bit / s}} = 0.5 * 10^{-15} / \text{bit}$$

This calculation demonstrates with a confidence level of 90% a BER below  $10^{-15}$  errors / bit.

Please note that this BER value is of statistical nature. The data is based on tests done on standard production boards. The BER is impacted by the quality of the application printed circuit board layout and its electrical environment. Inova Semiconductors can therefore not provide any guarantee on the BER obtained in a different application or a different electrical environment.

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