

APIX2 – a whole flood of data



Video, audio and Ethernet – all together now at 3 Gbit/s on one data highway

At the recent embedded world 2011 show in Nuremberg, Inova Semiconductors presented generation #2 of its automotive pixel link, which can transmit entirely different data formats on a single cable at 3 Gbit/s as far as 15 meters. APIX2 consequently not only shows the way to new display and driver assistance systems in automobiles. The multifunction link also opens up new possibilities for industrial displays.

By Robert Kraus

In 2007 Inova Semiconductors presented its first-generation APIX (automotive pixel link) scaled for 1 Gbit/s, and developed in collaboration with automaker BMW to match the requirements of an automotive environment – dependable data transmission paired with optimal EMC performance. Unlike comparable pixel links, APIX1 already was not simply intended as a display link to transmit just pixel data. On bidirectional communication channels APIX1 enabled a control unit to exchange data with a display, doing away with the need for an extra control bus.

APIX1 had its automotive premiere in the current BMW 7-series in November 2008. Since then it has gone into use millions of times over worldwide, and not only in an increasing number of vehicle models. Given its functionality and reliability, APIX1 has also appeared in a variety of industrial and medical applications, especially in camera-aided inspection and diagnostic systems.

APIX shows the dashboard

Even though the APIX1 data rate of 1 Gbit/s is adequate for most display formats, there is nevertheless a marked trend among premium carmakers towards substantially larger displays, able to show videos in HD quality for instance.

A single large 12-inch display with up to 1600 × 600 pixels resolution is set to replace the entire functionality – mechanical instruments and indicators – of a dashboard cluster. To present all the information here, including judder-free pointers in high quality, the link must be capable of transmitting at speeds up to 2.5 Gbit/s.

The new generation of high-resolution and high-contrast megapixel image sensors that are increasingly coming into use in modern driver assistance systems requires a fast gigabit-plus link to a graphics processor for uncontained implementation of their impressive imaging performance.

Today's new generation of graphics processors too, with their powerful

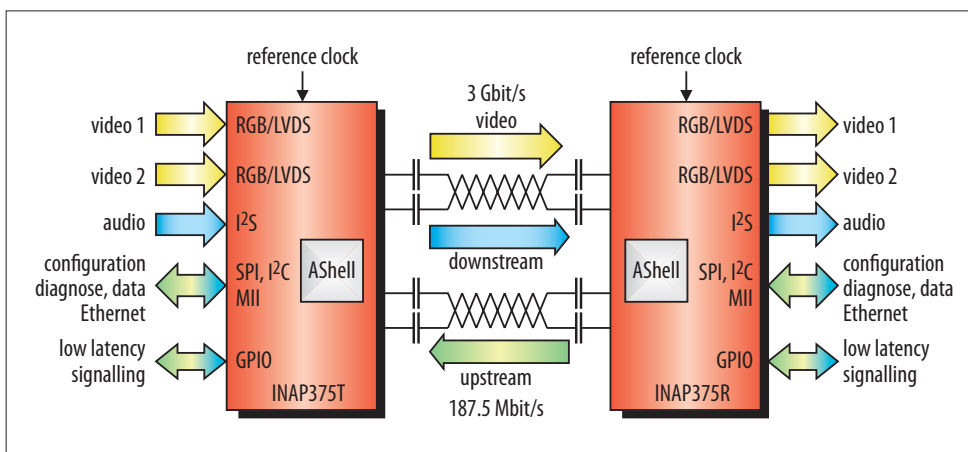


Fig. 1. Block circuit diagram of the transmitter and receiver modules INAP37T and INAP37R of APIX2.

APIX2 profile

- ▶ Compatible with APIX1
- ▶ Uninterrupted downstream data with 0.5 Gbit/s, 1 Gbit/s and 3 Gbit/s for video data rates up to 2.5 Gbit/s
- ▶ 187.5 Mbit/s and 62.5 Mbit/s bandwidth for uplink data stream
- ▶ Two independent video data streams
- ▶ Configurable video/data interface:
 - parallel RGB (10, 12, 18, 24 bits)
 - LVDS single- and dual-channel (18, 24 bits)
 - bulk data mode (16 bits and 2 flags)
- ▶ Video resolution up to:
 - 1920 × 1080 × 24 bits (1080i)
 - 1600 × 600 × 24 bits
 - 1280 × 1024 × 24 bits
- ▶ Configurable bidirectional communication, channels for two INAP37R receiver devices
- ▶ SPI data interface
- ▶ I²C master interface
- ▶ Media-independent interface (MI) for Ethernet
- ▶ GPIO with support for camera synchronization
- ▶ Embedded AShell
- ▶ I²C audio interfaces:
 - 16, 24 and 32 bits data formats
 - sampling frequencies 44.1 and 48 kHz
- ▶ TDM support for up to eight channels
- ▶ Diagnostic functionality:
 - selftest
 - embedded diagnostics
- ▶ Range up to 15 meters at 3 Gbit/s (wire: Ernst & Engring)
- ▶ Operating temperature range -40 to +105°C
- ▶ LQFP package with 100 pins

ARM Cortex cores, is able to process the data volume of a number of high-resolution cameras in parallel and in realtime, calling for a gigabit link scaled to reliably transport such huge quantities of data.

APIX2 – research project to start

To satisfy emerging demands and offer users, in APIX, a modern and future-oriented connectivity solution, Inova Semiconductors continued development into APIX2. Fully downward compatible with APIX1, it transmits up to 3 Gbit/s and enables a number of new features with its higher data rate (see Fig. 1 and Box).

Actually, development of APIX2 was headed by an extensive research project, sponsored in part by Germany’s Ministry of Education and Research (BMBF). Despite the bonus in data rate, industry wanted to be able to use the same materials, low-cost boards and copper wires as in the ready implemented 1 Gbit/s generation – without sacrificing reliability, ruggedness and range.

At this kind of data rate with a bit length of just 333 ps, parasitic effects of the copper wire produce extreme signal distortion (Fig. 2). Aimed at ensuring dependable data transmission, complex digital filter methods had to be devised for signal conditioning and implanted in the chips. New methods were also needed to simulate and compensate parasitic, crosstalk and other forms of interference.

APIX2 sets up on a special clock system of the kind already used in APIX1. This independent system

transports data constantly and continuously like a conveyor belt, but at different speeds in the two directions. Video signals and other data are trans-

mitted packet-oriented in frames – quite independently of the content or clock of the pixel signal (Fig. 3).

With APIX2 it is consequently pos-

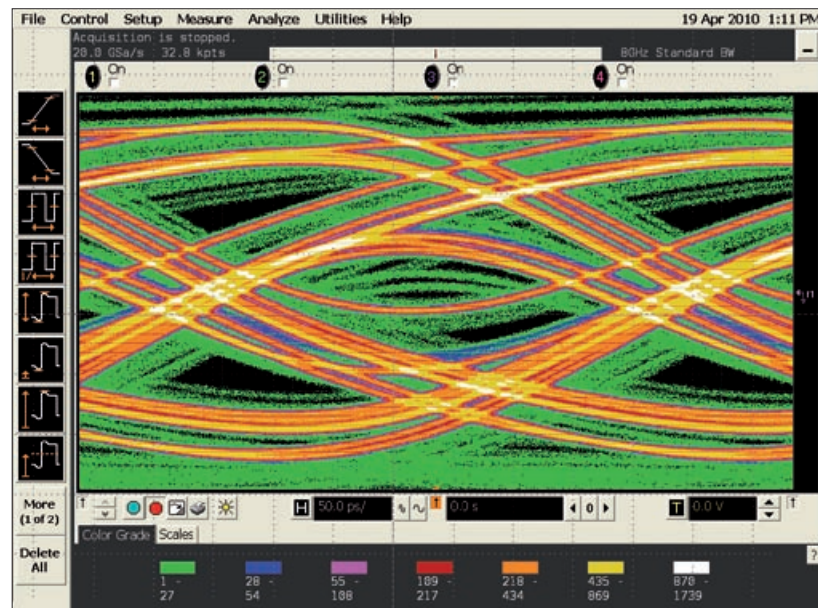


Fig. 2. Eye diagram of the 3 Gbit/s signal at the end of a 5-meter link, measured on an STP cable without active signal conditioning.

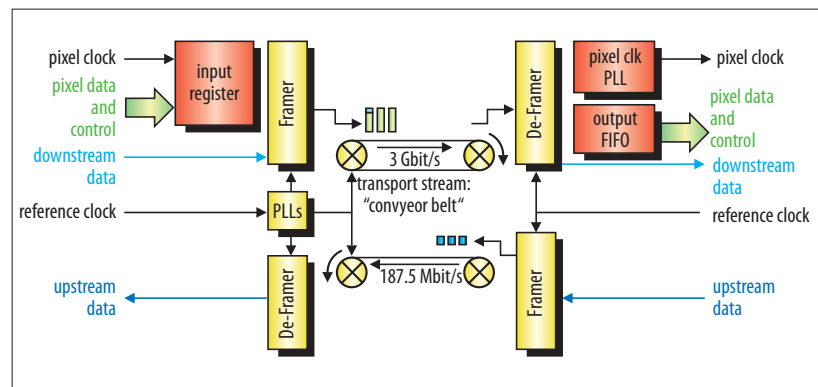


Fig. 3. Functional principle of the APIX link: Data are transmitted as on a conveyor belt in realtime – continuously in both directions and quite independently of image parameters or pixel clock jitter.

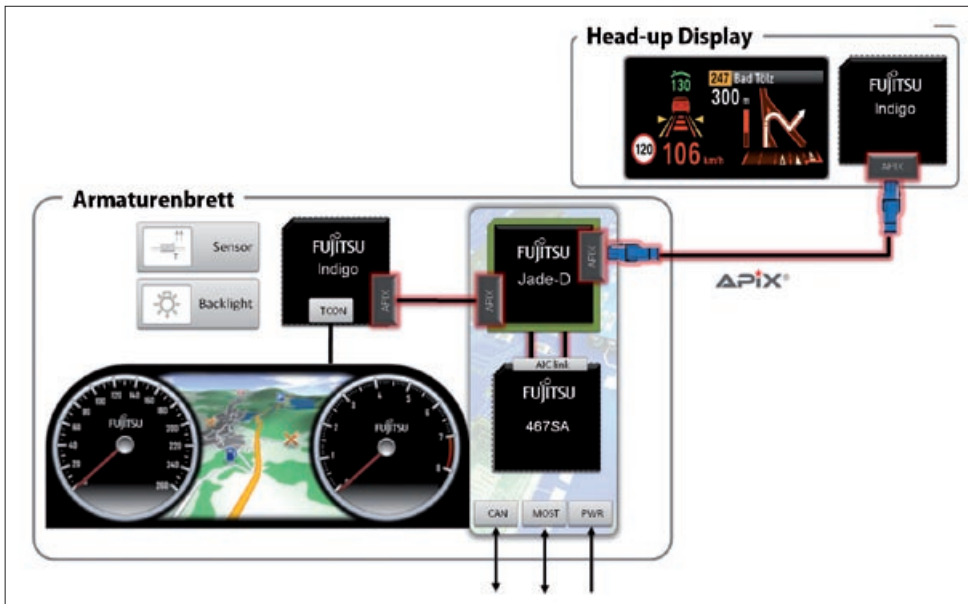


Fig. 4. Controller, graphics processor and graphics display controller with an integrated APIX1 interface in a dashboard. (picture: Fujitsu Semiconductor)

sible to simultaneously transmit two different video formats, digital multichannel audio and generic bus protocols like I²C on the bidirectional communication channels deterministically and practically in realtime. Innovative in APIX2 is the use of a standard-compliant MII (media-independent interface). A MAC controller can be directly connected here, so APIX2 can also work as an Ethernet link and transmit IP packets at 100 Mbit/s.

A protocol developed by Inova Semiconductors – called AShell or automotive shell – additionally guards these communication channels to transfer security-critical data.

Clever data coding

APIX2 revolves around its line code. This embeds all data within a frame

by a special method to ensure that – quite independently of video content and the other data transmitted – there is always a constant, regular data stream void of DC components.

This is a requirement not only for capacitive coupling of the cable but also for an evenly distributed RF spectrum in the serial data stream and thus minimal electromagnetic radiation. The intelligent coding of data in APIX2 also reduces overheads for error protection to a minimum. Instead of 25% or around 750 Mbit/s with conventional 8B/10B coding and 8-bit parity, APIX2 continuously produces about 2.8 Gbit/s net data throughput (payload) – with overhead of less than 8%.

The first alpha customers have already implemented APIX2 on their new multimedia platforms, due to go

into series production from early 2012. APIX2 chips are available now in batch quantities, and in ADK2 Inova Semiconductors can deliver a modular demo kit plus numerous other tools.

Discrete chip or even an SoC

APIX not only comes as a discrete link chip. From the very start Inova licensed the technology to other manufacturers, with the result that the APIX1 interface is integrated today in SoCs from Toshiba and Fujitsu Semiconductor (Fig. 4), and also serves as a soft core for Spartan-6 FPGAs from Xilinx. In Emerald P Fujitsu has now presented the world’s first graphics processor with no less than four integrated APIX2 interfaces. The central processing unit of this second SoC generation of the Emerald family is an ARM Cortex-A9 with NEON SIMD capability added on to process multimedia data. Nucleus of the chip is a 3D graphics unit supported by OpenGL ES 2.0 plus an independent 2D graphics engine. The three parallel display controllers each possess their own APIX2 interface to distribute video data uncompressed and in maximum resolution to the displays. That enables the chip to be used for a user-programmable or hybrid display panel showing high-resolution graphics. The other APIX2 outputs enable direct connection of a central display (CID) and a further display unit like a headup for instance.

On an additional APIX2 video input, data can be sent latency-free and in optimum digital quality from a head unit or camera to the Emerald P and processed there.

Three APIX2 transmitters and one receiver are integrated in this first Emerald P architecture. The modular approach makes for speedy implementation of other configurations, so the technology is also suitable for the emerging shift in driver assistance systems from analog to digital cameras.

Boom in camera-aided driver assistance

Makers of graphics processors are also looking into product concepts with a number of APIX2 receiver blocks on-board. Now that a Taiwan producer



Fig. 5. Full-digital 360° round-view driver assistance system with active pedestrian detection. (picture: DSP-Weuffen)

has already presented its first all-digital dual-chip camera modules with HD megapixel sensors from OmniVision and Aptina plus an APIX2 transmitter device, a graphics processor with four or more APIX2 inputs will be the next key product in the APIX portfolio.

This shows the way to economical implementation of powerful multiview camera systems that not only produce round-view pictures in perfect HD quality but also scan them and warn the driver, for instance, if a pedestrian suddenly crosses the road ahead of a vehicle.

Such camera-aided driver assistance systems are all set to boom in the near future. Experts forecast 400% growth in the imaging camera market in Europe and North America – especially as a result of new legal regulations – over the next five years. Systems with multiple cameras at 27% average annual growth will book a more than proportional share of this.

At embedded world 2011, as a lead-up to the planned full integration of a number of APIX2 receivers in one graphics processor, Inova Semiconductors together with NVIDIA and systems specialist DSP-Weuffen was already able to present a full-digital round-view system with pedestrian



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is co-founder and managing partner of Inova Semiconductors. After studying communications engineering in Munich he started his career at Motorola Semiconductors in 1986. He held management positions in various engineering sectors and in 1995 also assumed responsibility for establishing design centers and strategic cooperation in Eastern Europe. In 1997 he was appointed senior manager in the global development of new standard products for the automotive sector. Since Inova Semiconductors was founded in February 1999 he has managed the fortunes of the undertaking.

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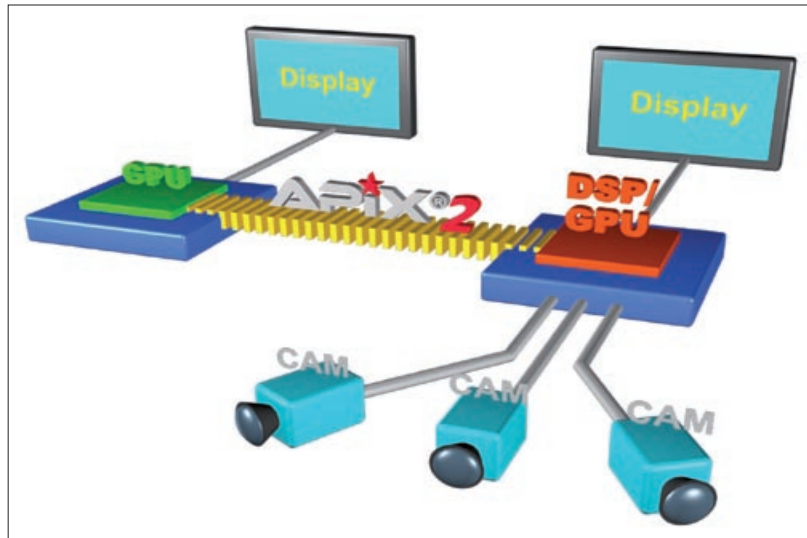


Fig. 6. Concept for networking display systems over APIX2 to distribute uncompressed video streams in realtime and securely exchange control data. (source: BMW)

detection in which four HD cameras with an OmniVision OV10630 HDR sensor are tied by APIX2 to an NVIDIA PC graphics system (Fig. 5).

■ Multimedia and data inflation in the automobile

Displays in automobiles are becoming larger as well as increasing in number. In future high-end or luxury models are going to have as many as six built-in displays, and partly networked with camera systems. Classic indication of speed, kilometer or mileage reading, fuel level, cooling water temperature and the like will be joined by high-resolution images from round-view and night vision systems, navigation with 3D graphics and information in a headup display in the windscreen.

The generation iPhone also expects its mobile companions to be able to use it unrestricted in the automobile. In addition to playing music or videos and accessing the internet and e-mail, it will soon be possible to customize the presentation on a display.

BMW, leading in the creation of modern multimedia and display concepts for automobiles, sees the solution in plain integration of functionality. Comments Dr Wolfgang Rieger, Manager of Driver Information Concepts, Software & Display Technology at BMW, „For cost reasons we'll also have greater density of integration, in other words today's functions in the smaller control units will be distributed among a certain number of power-

ful ECUs. The APIX2 bus thus takes on new importance in system architecture for networking displays, with special focus on video data streams.“

Fig. 6 is an example of a BMW concept in which two display systems are networked with one another over APIX2. In addition to distributing uncompressed video streams to the different displays in realtime, it enables a secure exchange of control data between the two processor units. APIX2 thus not only creates a system that can handle a large volume of video data. The architecture also plays a house-keeping role in dramatically increasing data throughput in a vehicle.

The development towards increasingly powerful multimedia applications in the automobile is set to continue. Controlling, trunking, channeling the resultant data streams will naturally be a central focus in automotive electronics. The demands of interior designers for a greater degree of freedom in creating the cockpit and dashboard will mean that certain control units have to surrender their accustomed niches and move into the trunk for instance. And that the number is reduced by substituting SoCs with their larger scale of integration. In APIX Inova Semiconductors and its partners are able to present a ready, viable concept for producing a variety of solutions. Generation APIX2 is by no means the end of the highway of course – thoughts at Inova Semiconductors are already turning to APIX next. *jk*