

GigaSTAR[®]

Frequently Asked Questions

Revision 1.4
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FAQ 1:

Is it possible to transfer data from a parallel bus completely asynchronously, or with a frequency below 33 MHz ?

Answer:

Yes, of course! The user controls the input data latching of the GigaSTaR Transmitter parallel interface through the VALID signal. When the VALID signal is set HIGH, the Transmitter will latch the data from the parallel bus and provide a clock pulse at RDCLK to indicate that the input data have been latched. The VALID signal can be asserted and de-asserted asynchronously. To support lower data rates just assert VALID each time when new data is available. After a rising edge of RDCLK in case no new data is available, VALID can be de-asserted until new data are available.

FAQ 2:

Will the GigaSTaR Receiver WRCLK follow precisely the frequency of assertion of the Transmitter's VALID input?

Answer:

Yes, the GigaSTaR Receiver WRCLK signal will follow the frequency of assertion of the Transmitter's VALID input. However, as the Transmitter's inputs are asynchronous and are sampled with a limited frequency, the Receiver's WRCLK signal will reproduce the frequency within a timesteps of 6ns.

For example, if the Transmitter VALID input is toggled with 32.99 MHz, the WRCLK of the Receiver will oscillate with 33MHz, periodically inserting a pause of 6ns, and continue to oscillate with 33MHz, such that the overall mean frequency equals to 32.99 MHz.

Another example: The Transmitter is running in BURST mode (means: VALID permanently HIGH). Then, VALID is pulled LOW to exit the burst mode (detailed timing see GigaSTaR datasheet t_5 and t_{10}), and is pulled back HIGH immediately after that, the WRCLK will generate a pause of 6 ns.

Please contact our support line in case you have more specific questions on this subject.

FAQ 3:

Can other STP-cables than the GORE GigaSTaR cables be used?

Answer:

Yes, it is possible to use other STP cable like e.g. CAT 5 and CAT 7 cables. With these cables, distances of 30m (patch cables) and 50m (installation cables) are achievable. Different cable types may require modified line termination values at the GigaSTaR Receiver, please contact our support line at cs@inova-semiconductors.de in case you have a specific question.

FAQ 4:

Can other link media than STP-cable be used?

Answer:

Yes, this is possible! Coax cables as well as impedance controlled transmission lines can be used. Please note that both lines have to have exactly the same length and the impedance must match 50 Ohm single ended or 100 Ohm differential. Also, the line termination value at the GigaSTaR Receiver has to be matched, please contact our support line for details.

FAQ 5:

How can I build up an optical data transmission with fibre optic cable?

Answer:

The GigaSTaR can be directly connected to many optical gigabit transceivers. For details please see our Application Note "ING_IFM_AN". A convenient way is also to evaluate our ready-to-go fiber-optical piggyback board ING_TRF.

FAQ 6:

Can I use other connectors than the SUB-D9 connector which is mounted on the GigaSTaR piggyback boards ?

Answer:

Yes, there are many connectors which can be used. However, not all connectors, not even all SUB-D9 connectors, perform equally. The connectors should provide a differential impedance close to 100 Ohm, and their transmission performance should be investigated.

FAQ 7:

Does the GigaSTaR link automatically synchronise ?

Answer:

Yes! Each time the VALID signal is LOW, the GigaSTaR Transmitter will insert stuffing patterns into the serial data stream to keep the Receiver PLL in sync. These stuffing patterns will re-synchronise the link within 25 us (worst case) if the PLL was not unlocked, see also FAQ7. Please note: toggling VALID with 33MHz has the same effect like keeping it permanently high – the link operates in BURST mode. To enable the insertion of stuffing patterns, VALID has to be toggled with less than 33MHz.

FAQ 8:

In case of transmission errors, does the GigaSTaR link automatically synchronise?

Answer:

Yes! If the serial transmission contains stuffing patterns (see FAQ 6), the GigaSTaR link will have deterministic re-synchronisation times: 25µs after a bit error which has not corrupted the frame structure and 125µs in case the PLL was unlocked. If the serial data does not contain stuffing patterns, the link typically becomes synchronous but not within a deterministic time.

FAQ 9:

What is the worst case time to correct data transmission after a reset pulse ?

Answer:

The worst case reset recovery time for the Receiver is 125µs.

FAQ 10:

Is it possible to use other reference clock frequencies than the 66MHz specified in the data sheet ?

Answer:

Lab testing with various oscillator frequencies showed that at 25°C, the PLL will typically lock on all clock frequencies between 60 and 70MHz. The PLL locking range is dependent on the chip temperature as well as on processing parameters. Therefore, PLL locking in the 60 MHz - 70 MHz range is expected but neither tested nor guaranteed. A guarantee for PLL locking is only given for the frequency and temperature range as specified in the ING165B_DS data sheet.

FAQ 12:

In which state is the FLAGO output after a reset pulse?

Answer:

After reset, the FLAGO output will be in LOW state.

FAQ 12:

What is the typical bit error rate (based on pseudo-random pattern) of a GigaSTaR link with 20m-30m length without any error-correcting protocol?

Answer:

In a properly designed GigaSTaR link (with cable type, connectors and line termination properly matched), bit error rates of 10E-14 and better are typical.

FAQ 13:

What is the purpose of the equalizer function of the GigaSTaR RX device?

Answer:

The equalizer function allows to compensate for the frequency-dependant transmission cable attenuation. For transmission cable lengths above 10 m (this value refers to the GORE reference cable GGSC1608-X, other cable types may differ), it is recommended to activate the equalizer function to achieve optimum transmission stability and bit error rate.

FAQ 14:

What does "GigaSTaR easy-to-use interface" mean?

Answer:

This means that the GigaSTaR link does not require any complicated adaptation at its parallel interface. Instead, a simple handshake mechanism has been implemented to allow an easy use of the GigaSTaR link: to transmit the 36 data bits to the Receiver, just pull the VALID signal high. For more details and timing specifications, please refer to the ING165B_DS data sheet.

FAQ 15:

Is it possible to exchange the serial line signal SDATA with $\overline{\text{SDATA}}$ (inversion of SDATA)?

Answer:

No, this would not only cause data inversion but also destroy header information which is required to keep the link synchronised.

FAQ 16:

What is the minimum differential swing for the serial inputs GigaSTaR Receiver?

Answer:

The typical (not tested nor guaranteed) minimum differential swing for the serial inputs of the GigaSTaR Receiver is 120mV @ 25°C and 3,3V Vcc.

FAQ 17:

What makes the GigaSTaR transmission link so robust?

Answer:

Thanks to the efficient data and header coding, the GigaSTaR got only 10% code overhead (compared to 20%...50% of comparable links). This allows transmitting the same amount of payload data at a lower serial RF frequency than other links. Together with the excellent PLL and RF characteristics of the GigaSTaR's ECL circuits, it enables the GigaSTaR to achieve very long transmission distances with copper cables (>50m) and superb bit error rates (<10E-14).

FAQ 18:

Is it possible to further increase the transmission distance if a lower payload data rate than the 1.188Gbit/s is used?

Answer:

No – the GigaSTaR serial link always operates in its optimised RF frequency band, independent from the amount of payload data. Therefore the achievable link distance is not a function of the amount or frequency of payload data.

FAQ 19:

Is it required to force a reset pulse after a LOCK or LSYNC# pulse?

Answer:

Generally not. A LSYNC# pulse indicates a bit error while a LOCK pulse indicates a catastrophic event like cable breakage or extreme power/ground bounce. However, the GigaSTaR should re-synchronise itself through the resynchronization patterns, which are generated regularly by the Transmitter if the frequency at the VALID input is below 33MHz (see also FAQ 6 and 7).

If the GigaSTaR link operates in BURST mode (VALID permanently high or toggled with 33MHz) then pulling VALID low for 125µs will ensure resynchronization even after a catastrophic event.

FAQ 20:

Which device should I power up first, the Transmitter or the Receiver?

Answer:

If the insertion of stuffing pattern is enabled (toggle VALID with less than 33Mhz, see FAQ 6), then no power-up sequence or procedure is required for power-up – the automatic re-synchronization will take care for the link synchronization.

If VALID is permanently high or toggled with 33MHz, no ordering is required as long as it is guaranteed that VALID at the Transmitter is low until the LSYNC# signal at the Receiver goes low. If no feedback channel is available to provide the LSYNC# status, please use following power-up sequence:

Power up the Receiver first (at least not later than the Transmitter) and activate the reference clocks for both devices. Set RESET# low on Transmitter and Receiver for at least 2ms after power-up and keep VALID at the Transmitter low for 125µs after the reset is released. The Receiver will lock properly.

FAQ 21:

Which significance have the rise & fall times at the parallel input of the Transmitter?

Answer:

The rise & fall times at the parallel input of the Transmitter have not been noticed to have a huge impact. It is however important to control over & undershoots and to respect the correct setup & hold timing. Violation of the setup & hold timing can cause the input interface to become frozen.

FAQ 22:

Can I supply the different supply voltages from different power sources?

Answer:

It is highly disrecommended to supply the different supply voltages from different power sources, because these may have different ramping characteristics during power up and power down sequences. If one supply node is ramped faster than another, cross-currents through VDD / GND pins may exceed the maximum ratings and cause damage to the device. Please check the maximum ratings and handling precautions in the ING165B_DS data sheet.

FAQ 23:

Are layout data for a GigaSTaR PCB layout available?

Answer:

Yes, the layout data for a GigaSTaR PCB layout are available in pdf and Gerber format on request, please contact our support line at cs@inova-semiconductors.de .

FAQ 24:

What exactly is happening during the Transmitter and Receiver locking process?

Answer:

The GigaSTaR Transmitter and Receiver PLL need approximately 2 ms to become frequency locked after the reference clock of 66 MHz is enabled. This process is not influenced by reset, it just starts as soon as the reference clock is available.

As soon as the Transmitter PLL is locked, the LOCK signal goes to 1. Assuming the Transmitter PLL is frequency locked, it takes further 50 μ s after reset was deasserted until the Transmitter is in an operational mode. During this time, the device holds its internal reset active and no data is transmitted. When the device is in operational mode and if VALID = 0, synchronization patterns are transmitted, otherwise data is transmitted. In case of the very unlikely event that an unlock conditions happens (LOCK= 0) the Transmitter goes through the same sequence, and 50 μ s after LOCK = 1 the Transmitter goes back to the operational state.

The Receiver goes through a 2 step locking process. First, similar to the Transmitter, the Receiver PLL does a frequency lock as soon as the reference clock is enabled (2 ms). The Receiver remains in the frequency locking process until the PLL is properly frequency locked and reset is deasserted. After reset was deasserted, 50 μ s later the Receiver starts to lock on the incoming data stream. If no data is provided (for example, if the Transmitter is still not operational), the PLL will loose frequency lock and as a consequence the Receiver starts the frequency locking process again until it is locked.

If data is provided, the PLL locks on the incoming data. This might cause LOCK = 0 pulses, but not necessarily. 50 μ s after LOCK = 1 the Receiver is locked to the incoming data stream. In case of the very unlikely event that an unlock condition occurs (LOCK = 0), the Receiver goes through the same sequence. 50 μ s after LOCK = 1 the Receiver is frequency locked and further 50 μ s after LOCK = 1 the Receiver is locked to the incoming data.

Now, earliest 100 μ s after reset was deasserted or an unlock condition has occurred, the Receiver is properly locked to the incoming data stream.

After being data locked, the Receiver releases the internal reset and starts to look for the frame structure within the serial data stream. If synchronization patterns are received (Transmitter VALID = 0, see FAQ 6), this process takes 25 μ s. If data is provided at this time (Transmitter VALID=1 or toggled with 33MHz, see FAQ 6), this process is not deterministic and might cause the Receiver never to become frame synchronous, what means the frame structure was not properly detected and LSYNC# stays at 1.

After the Receiver was frame synchronous one time, it will become frame synchronous again after a loss of frame synchronization due to bit errors (LSYNC # =1), even if data patterns are provided.

Only if a unlock has happened and after reset, the Receiver requires synchronization patterns (VALID=0) to become frame synchronous.

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